D. Y. Patil College of Engineering, Akurdi, Pune-44
Department of Electronics & Telecommunication

Date: 04/12/2020

Following is the Timetable for Backlog (Elective I) Online examination of April/ May- 2020 for ME- E&TC, VLSI & Embedded System (2017 Pattern):

Sr. No	Course Name	Subject Code	Subject Name	Year	Semester	Exam Date	Time Slot
1	ME-2017 Pattern	504205	Elective I- Processor Design	ME 1st Year	I	9/12/2020	10:00 AM to 2:00 PM

4/12/2020
Dr. D. G. Khairnar
Prof. & HOD E&TC

Dr. Vijay M. Wadhai
Principal