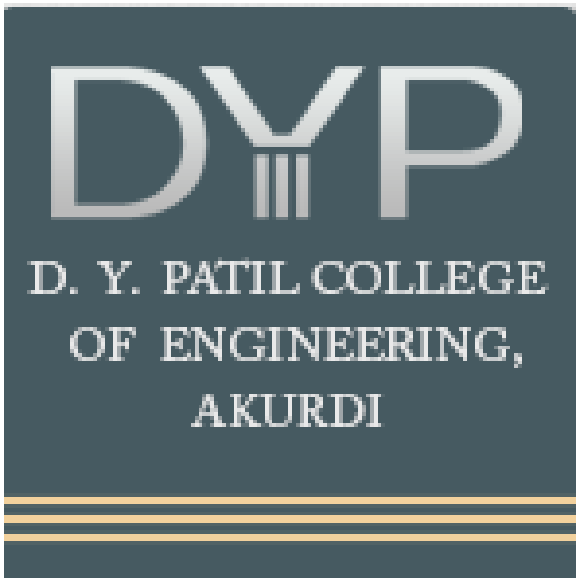
**D. Y. Patil College of Engineering, Akurdi**

**Department of Electronics & Telecommunication**

**Academic Year 2024-2025**




# M.Tech VLSI and Embedded System

## Syllabus Copy

# D Y Patil College of Engineering, Akurdi, Pune

An Autonomous Institute from AY 2024-25, Affiliated to Savitribai Phule Pune University, Pune

**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester I

## Syllabus Structure

| Course Code | Course | Teaching Scheme | | | | Evaluation Scheme | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | L | T | P | Cr | Exam | Theory % Marks | | | Practical % Marks | |
| | | | | | | | Max | Min for Pass | | Max | Min for Pass |
| VES2409L01 | Digital CMOS Design | 3 | 1 | 0 | 4 | CCA | 50 | 20 | 40 | - | - |
| | | | | | | ESE | 50 | 20 | | | |
| VES2409L02 | Embedded System Design | 3 | 1 | 0 | 4 | CCA | 50 | 20 | 40 | - | - |
| | | | | | | ESE | 50 | 20 | | | |
| VES2409L03 | Reconfigurable Computing | 3 | 1 | 0 | 4 | CCA | 50 | 20 | 40 | - | - |
| | | | | | | ESE | 50 | 20 | | | |
| VES2409LXX | Program Elective Course 1 | 3 | 1 | 0 | 4 | CCA | 50 | 20 | 40 | - | - |
| | | | | | | ESE | 50 | 20 | | | |
| VES2409P01 | Laboratory Practice I | 0 | 0 | 4 | 2 | CCA | - | - | - | 50 | 20 |
| | | | | | | ESE | - | - | - | 50 | 20 |
| RMD24O9L01 | Research Methodology | 3 | 0 | 0 | 3 | CCA | 50 | 20 | 40 | - | - |
| | | | | | | ESE | 50 | 20 | | | |
| VES2409P02 | Research Seminar | 0 | 0 | 2 | 1 | CCA | - | - | | 50 | 20 |
| | | | | | | ESE | | | | 50 | 20 |
| NCC2409L01 | Non Credit Course 1 | 2 | 0 | 0 | 0 | CCA | 100 | 40 | | Pass/Fail | |
| **Total** | | **17** | **4** | **6** | **22** | | | | | | |

| **Program Elective Course 1** | |
|---|---|
| VES2409L04 | ASIC Design |
| VES2409L05 | Nano Technology |
| VES2409L06 | Processor Design |
| VES2409L07 | Wireless Sensor Networks |
| VES2409L08 | Industrial IOT in Embedded system |

| **Non Credit Course 1** | |
|---|---|
| NCC2409L01 | Disaster Management |
| NCC2409L02 | Value Education |
| NCC2409L03 | Constitution of India and Indian Knowledge System |
| NCC2409L04 | Pedagogy Studies |

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester I

**Category: Program Core Course 1**

| Teaching Scheme | | | | Evaluation Scheme | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| L | T | P | Cr | Exam | Theory % Marks | | | Practical % Marks | |
| | | | | | Max | Min for Pass | | Max | Min for Pass |
| 3 | 1 | 0 | 4 | CCA | 50 | 40 | 40 | | |
| 39 | 13 | 0 | Total:52 | ESE | 50 | 40 | | | |

**Course Code: VES2409L01** **Course Title: Digital CMOS Design**

**Prerequisites:**
1. Basic understanding of MOSFETs
2. Basic fundamentals of integrated circuits.

**Course Objectives:**

1. To learn MOSFET Models and layout fundamentals
2. To nurture students understanding in performance parameters of digital CMOS Design
3. To understand the advanced trends in CMOS design
4. To learn the delay models

**Course Outcomes:** After successful completion of the course the student will be able to:

| | |
|---|---|
| CO1 | Apply the knowledge of electrical properties, characteristics and capacitance models of MOSFET to design its SPICE Model. |
| CO2 | Design digital logic circuits using CMOS technology and draw and simulate the CMOS layout of digital circuits. |
| CO3 | Analyze various performance parameters of CMOS and estimate the delay of logic networks and its logical efforts in digital CMOS design. |
| CO4 | Design, simulate and synthesize CMOS combinational and sequential circuits HDL codes using FSM and analyze the performance. |
| CO5 | Design low power and high speed circuits with comparative understanding of circuit families and advanced circuits. |

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester I

## Syllabus

| | | |
|---|---|---|
| **Unit I** | **Title: MOSFET Models** | **8 hrs** |
| Basic Electrical Properties of MOS Circuits: Ids-Vds Relationships, MOS Transistor Threshold Voltage Vth, MOS Capacitance models, MOS Gate Capacitance Model, MOS Diffusion Capacitance Model. Non ideal I-V Effects, MOSFET equivalent circuits and analysis, Parasitic; Technology scaling; Lambda parameter; wiring parasitic; SPICE Models | | |
| **Unit II** | **Title: CMOS Layout Techniques** | **8 hrs** |
| CMOS layout techniques; Transient response. CMOS Technologies: Layout Design Rules CMOS Process Enhancements: Transistors, Interconnect, Circuit Elements, Beyond Conventional CMOS. CMOS Fabrication and Layout: Inverter Cross-section, Fabrication Process, Stick Diagrams. | | |
| **Unit III** | **Title: Performance parameters** | **8 hrs** |
| Static, dynamic and short circuit power dissipations, Propagation delay, Power delay product, Fan in, fan out and dependencies. Delay Estimation**:** RC Delay Models, Linear Delay Model, Logical Effort, Parasitic Delay. Logical Effort and Transistor Sizing: Delay in a Logic Gate, Delay in Multistage Logic Networks, Interconnect: Resistance, Capacitance, Delay, Crosstalk. Design Margin. | | |
| **Unit IV** | **Title: Logic design and FSM Design with issues** | **8 hrs** |
| Static CMOS Logic: Inverter, NAND Gate, Combinational Logic, NOR Gate, Compound Gates, Pass Transistors and Transmission Gates, Tristates, Multiplexers, Latches and Flip-Flops, Design calculations for combinational logic and active area on chip; Hazards, sources and mitigation techniques, Transmission gate, utility and limitations.<br>Concepts of FSMs, Types of FSMs, Basic design approach, HDL codes for FSM, Metastability issues and solutions; Timing analysis, Design Examples, Simulation and Synthesize using HDL | | |
| **Unit V** | **Title: Advanced tends** | **7 hrs** |
| Circuit Families**:** Static CMOS, Ratioed Circuits, Cascode Voltage Switch Logic, Dynamic Circuits, Domino logic, NORA logic, Differential Circuits, Sense Amplifier Circuits, BiCMOS Circuits, Low Power Logic Design, Comparison of Circuit Families, Materials for performance improvement, Techniques for Low power, High speed designs. | | |
| **Reference Books** | | |
| | | |

## FY M Tech VLSI and Embedded Systems, Semester I


1. Neil Weste and Kamaran, ―Principles of CMOS VLSI Design‖, Education Asia.
2. M. Rabaey, A. Chandrakasan and B. Nikolic, Digital Integrated Circuits : A Design Perspective, Pearson (Low Price Edition)
3. Charls Roth, ―Digital System Design using VHDL‖, Tata McGraw Hill.
4. S-M. Kang and Y. Leblebici, CMOS Digital Integrated Circuits : Analysis and Design, Third Edition, McGraw-Hill
5. Samir Palnitkar, ―Verilog HDL – A Guide to Digital Design and Synthesis‖, PHI


**Tutorial**

| | | |
|---|---|---|
| **Unit I** | **Title: MOSFET Models** | **3 hrs** |
| 1. Design SPICE model of MOSFET and explain the steps in detail.<br>2. Justify significance of non-ideal V-I Characteristics and parameters of MOSFET.<br>3. Justify wiring parasitic and device parasitic limitations on speed and bandwidth of the MOSFET circuit. | | |
| **Unit II** | **Title: CMOS Layout Techniques** | **2 hrs** |
| 1. Design CMOS circuit using layout design rules with any one example.<br>2. Relate the CMOS fabrication process and draw the stick Diagram. | | |
| **Unit III** | **Title: Performance parameters** | **3 hrs** |
| 1. Analyze effect of static, dynamic and short circuit power dissipations in the CMOS circuits.<br>2. Relate and express significance of Fan-in, Fan-out and power delay product in CMOS circuit designing. What are the ways to improve them? | | |
| **Unit IV** | **Title: Logic design and FSM Design with issues** | **3 hrs** |
| 1. Design CMOS circuit for Y = AB + CDEF + GH. Carry out the transistor sizing.<br>2. What is the effect on logic ―1‖ and ―0‖ if Pull-Up and Pull-Down networks are made up of N and P devices respectively in CMOS logic? Give example. | | |

## FY M Tech VLSI and Embedded Systems, Semester I

| | | |
|---|---|---|
| 3. Design HDL code for FSM. Explain it in detail with suitable examples.<br>4. Demonstrate the solution of Metastability issues in FSM designs. | | |
| **Unit V** | **Title: Advanced trends** | **2 hrs** |
| 1. Compare circuit families with their performance parameters<br>2. Design circuit with Cascode Voltage Switch Logic and draw its timing diagram. | | |

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester I

### Rubrics for Continuous Evaluation

| Component | Level | Unit 1 | Unit 2 | Unit 3 | Unit 4 | Unit 5 | Total | Process Evaluation |
|---|---|---|---|---|---|---|---|---|
| Continuous Comprehensive Assessment (CCA) | Faculty | 10 | 10 | 10 | 10 | 10 | 50 | Refer CCA Guideline |
| End Semester Examination (ESE) | Institute | 10 | 10 | 10 | 10 | 10 | 50 | Each Unit Carries 10 marks Question |

### CO-PO Mapping

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 3 | 2 | 3 | 2 | 1 | 1 |
| **CO2** | 3 | - | - | 2 | 1 | 1 |
| **CO3** | 3 | 2 | 2 | 1 | - | 1 |
| **CO4** | 3 | 2 | 2 | 2 | 2 | 1 |
| **CO5** | 3 | 2 | 1 | 1 | 1 | - |

3: High, 2: Moderate, 1: Low, 0/-: No Mapping

# D Y Patil College of Engineering, Akurdi, Pune

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester I

**Category: Program Core Course 2**

**Course Code: VES2409L02** **Course Title: Embedded System Design**

| Teaching Scheme | | | | Evaluation Scheme | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| L | T | P | Cr | Exam | Theory % Marks | | | Practical % Marks | |
| | | | | | Max | Min for Pass | | Max | Min for Pass |
| 3 | 1 | 0 | 4 | CCA | 50 | 40 | 40 | | |
| 39 | 13 | 0 | Total:52 | ESE | 50 | 40 | | | |

| | |
|---|---|
| **Prerequisites:** Basics of Embedded system | |
| **Course Objectives:** | |
| 1. To understand various design issues in embedded systems<br>2. To learn ARM CORTEX architecture and its programming concepts<br>3. To learn embedded LINUX operating system<br>4. To make aware of the significance of embedded network processors | |
| **Course Outcomes:** After successful completion of the course the student will be able to: | |
| CO1 | Appraise knowledge about the basic functions of embedded systems. |
| CO2 | Design ARM Processor based Embedded Systems. |
| CO3 | Select CORTEX based controller for suitable application and Interface the advanced peripherals to ARM based microcontrollers. |
| CO4 | Examine different booting and kernel methods for sustainable embedded system design. |
| CO5 | Develop Embedded C or C++ programming for embedded system design. |

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## FY M Tech VLSI and Embedded Systems, Semester I

## Syllabus

| | | |
|---|---|---|
| **Unit I** | **Title: Introduction to Embedded Systems** | **7 hrs** |
| Introduction to Embedded Systems: Introduction to Embedded Systems, Architecture of Embedded System, Design Methodology, Design Metrics, General Purpose Processor, System On chip. | | |
| **Unit II** | **Title: Embedded system design and development** | **8 hrs** |
| Embedded system design and development**:** Embedded system design, Life-Cycle Models, Development tools, Introduction to Development Platform Trends (only introduce IDE, board Details and Application) Arduino, Beagle bone, Rasberry PI, Intel Galileo Gen 2. | | |
| **Unit III** | **Title: ARM CORTEX Processor and ARM-M3 Based Microcontroller** | **8 hrs** |
| ARM CORTEX series features, Improvement over classical series, CORTEX ARM processors series, Features and applications, Survey of CORTEX based controllers from various manufacturers.<br>ARM-M3 Based Microcontroller LPC1768: Features, Architecture block diagram & its description, System Control, Clock & Power Control, Pin Connect Block. CMSIS Standard, Bus Protocols Ethernet, CAN, USB, Bluetooth. | | |
| **Unit VI** | **Title: Embedded Linux** | **8 hrs** |
| Embedded Linux: System architecture, BIOS versus boot-loader, Booting the kernel, Kernel initialization, Space initialization, Boot loaders and Storage considerations. Linux kernel construction: Kernel build system, Obtaining a custom Linux kernel, File systems, Device drivers, Kernel configuration. | | |
| **Unit V** | **Title: Embedded System Design Case Studies** | **8 hrs** |
| Embedded System Design Case Studies: Design Case Studies like Automated Meter Reading Systems (AMR), Digital Camera, Certification and documentation: Mechanical Packaging, Testing, reliability and failure analysis, Certification (EMI / RFI) and Documentation. Study of any two real life embedded products in detail. | | |
| **References/Reference Books** | | |
| 1. www.nxp.com/documents/user, manual/UM10360.pdf.<br>2. Noergaard Tammy, ―Embedded Systems Architecture‖, Elsevier Publication.<br>3. Hallinan Christopher, ―Embedded Linux Primer: A Practical Real-World Approach‖, Second Edition, Pearson Education.<br>4. Shibu,‖ Introduction to Embedded Systems‖, TMH.<br>5. Comer D E, ―Network System Design using Network Process‖, PHI. | | |

6. Croeley Patrick, Franklin M. A, Hadimioglu H & Onufryk P Z,‖ Network Processor Design, Issues and Practices‖, vol-1-2, Elsevier.
7. Uyless Black,‖ Computer Networks-Protocols, Standards Interfaces‖, Second Edition,PHI.
8. http://www.npforum.org/; http://www.intel.com/design/network/products/npfamily.


**Tutorial**

| | | |
|---|---|---|
| **Unit I** | **Title: Introduction to Embedded Systems** | **2 hrs** |
| 1. With a neat sketch explain the Embedded Systems Architecture and appraise the system on chip concept. | | |
| **Unit II** | **Title: Embedded system design and development** | **2 hrs** |
| 2. Compare Arduino, Beagle bone, Raspberry PI and Intel Galileo Gen 2. | | |
| **Unit III** | **Title: ARM CORTEX Processor and ARM-M3 Based Microcontroller** | **3 hrs** |
| 3. Conduct Extensive Survey of CORTEX based controllers from various manufacturers.<br>4. With neat sketch explain LPC1768: Features, Architecture block diagram & its description. | | |
| **Unit IV** | **Title: Embedded Linux** | **3 hrs** |
| 5. Examine different booting and kernel methods for sustainable embedded system design. | | |
| **Unit V** | **Title: Embedded System Design Case Studies** | **3 hrs** |
| 6. Design Case Study on Embedded system like Automated Meter Reading Systems, (AMR), Digital Camera. | | |

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## FY M Tech VLSI and Embedded Systems, Semester I
## Rubrics for Continuous Evaluation

| Component | Level | Unit 1 | Unit 2 | Unit 3 | Unit 4 | Unit 5 | Total | Process Evaluation |
|---|---|---|---|---|---|---|---|---|
| Continuous Comprehensive Assessment (CCA) | Faculty | 10 | 10 | 10 | 10 | 10 | 50 | Refer CCA Guideline |
| End Semester Examination (ESE) | Institute | 10 | 10 | 10 | 10 | 10 | 50 | Each Unit Carries 10 marks Question |

### CO-PO Mapping

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 3 | 2 | 3 | 2 | 1 | 1 |
| **CO2** | 3 | - | - | 2 | 1 | 1 |
| **CO3** | 3 | 2 | 2 | 1 | - | 1 |
| **CO4** | 3 | 2 | 2 | 2 | 2 | 1 |
| **CO5** | 3 | 2 | 1 | 1 | 1 | - |

3: High, 2: Moderate, 1: Low, 0/-: No Mapping

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester I

**Category: Program Core Course 3**

**Course Code: VES2409L03** **Course Title: Reconfigurable Computing**

| Teaching Scheme | | | | Evaluation Scheme | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| L | T | P | Cr | Exam | Theory % Marks | | | Practical % Marks | |
| | | | | | Max | Min for Pass | | Max | Min for Pass |
| 3 | 1 | 0 | 4 | CCA | 50 | 40 | 40 | | |
| 39 | 13 | 0 | Total:52 | ESE | 50 | 40 | | | |

**Prerequisites:** Basics of VLSI design Flow, Basics of FPGA

**Course Objectives:**

1. To understand various computing architectures
2. To provide students the concept of handling issues of reconfigure computing
3. To provide students implementation approaches of FPGA design in view of reconfiguration
4. To outline various applications reconfigure computing

**Course Outcomes:** After successful completion of the course the student will be able to:

| | |
|---|---|
| CO1 | Compare and contrast the reconfigurable computing and its integration on computing platforms with general purpose, domain specific and application specific processors. |
| CO2 | Explore and apply different building blocks for RC Architectures. |
| CO3 | Analyze various systems of Reconfigurable computing and recognize their issues. |
| CO4 | Analyze and apply various reconfiguration management aspects. |
| CO5 | Design, implement and analyze reconfigurable systems in the recent application domains using HDL |

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## FY M Tech VLSI and Embedded Systems, Semester I

## Syllabus

| | | |
|---|---|---|
| **Unit I** | **Title: Domain of RC** | **7 hrs** |
| General overview of computing models, Basic RC concepts, Domain of RC: General Purpose Computing, Domain-Specific Processors, Application-Specific Processors, Reconfigurable Computing, Fields of Application. | | |
| **Unit II** | **Title: RC Architectures** | **8 hrs** |
| Architecture of Field Programmable Gate Arrays, Reconfigurable Processing Fabric (RPF) Architectures: Fine grained, Coarse-Grained, Integration of RPF into Traditional Computing Systems. | | |
| **Unit III** | **Title: Systems of Reconfigurable Computing** | **8 hrs** |
| Early systems of Reconfigurable computing: PAM, VCC, Splash, PRISM, Tera mac, Cray, SRC, non-FPGA research, challenges or post synthesis issues in systems of RC. | | |
| **Unit IV** | **Title: Reconfiguration Management** | **8 hrs** |
| Reconfiguration Management: Reconfiguration, Configuration architectures, managing reconfiguration process, reducing reconfiguration time, configuration security. | | |
| **Unit V** | **Title: Implementation of RC with Applications** | **8 hrs** |
| Implementation: Integration, FPGA Design Flow, System On A Programmable Chip: Introduction to SoPC, Adaptive Multiprocessing on Chip. Reconfiguration Project Design Approaches: J-Bit, Modular, Early Access, Vivado.<br>RC Applications (any three): Implementing applications with FPGAs, various applications and use of reconfiguration: Video Streaming, Distributed arithmetic, Adaptive Controller, Adaptive cryptographic systems, Software Defined Radio, High-Performance Computing, Automatic target recognition systems. | | |
| **Reference Books** | | |
| 1 Bobda Christophe, ―Introduction to Reconfigurable Computing: Architectures, Algorithms, and Applications‖, Springer.<br>2 Hauck Scott, Dehon A, ―Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation‖, Elsevier.<br>3 Vivado Partial Reconfiguration.pdf: user guide 909 by Xilinx Revision: 04/06/2016. | | |

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester I

**Tutorial**

| | | |
|---|---|---|
| **Unit I** | **Title: Domain of RC** | **3 hrs** |
| 1. State and explain reconfigurable device characteristics<br>2. Explain flow of program execution for Von Neumann computer architecture.<br>3. Compare & contrast between General Purpose Processors, Domain-Specific Processors, Application-Specific Processors, | | |
| **Unit II** | **Title: RC Architectures** | **2 hrs** |
| 1. Elaborate Garp's non-symmetrical RPF as fine-grained architecture<br>2. Compare Fine grained & Coarse-Grained fabrics in FPGA. | | |
| **Unit III** | **Title: Systems of Reconfigurable computing** | **2 hrs** |
| 1. Explain PAM as Reconfigurable computing with example<br>2. Analyze different research challenges in the design and development of Reconfigurable devices? | | |
| **Unit IV** | **Title: Reconfiguration Management** | **3 hrs** |
| 1. Compare & contrast between Programmable, configurable & reconfigurable architectures<br>2. Elaborate on Relocation and Defragmentation form RC point of view<br>3. What is Rent Rule? Explain its importance. | | |
| **Unit V** | **Title: Implementation of RC with applications** | **3 hrs** |
| 1. Elaborate with help of diagram the transfer of System from PCB to System on Programmable chip.<br>2. Explain J-Bit as Reconfiguration Project Design Approach.<br>3. Draw the architecture of adaptive controller ad explain it for control of complex Mechatronics system.<br>4. Elaborate Reconfigurable Computing for Software Defined Radio. | | |

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## FY M Tech VLSI and Embedded Systems, Semester I

### Rubrics for Continuous Evaluation

| Component | Level | Unit 1 | Unit 2 | Unit 3 | Unit 4 | Unit 5 | Total | Process Evaluation |
|---|---|---|---|---|---|---|---|---|
| Continuous Comprehensive Assessment (CCA) | Faculty | 10 | 10 | 10 | 10 | 10 | 50 | Refer CCA Guideline |
| End Semester Examination (ESE) | Institute | 10 | 10 | 10 | 10 | 10 | 50 | Each Unit Carries 10 marks Question |

### CO-PO Mapping

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 3 | 2 | 3 | 2 | 1 | 1 |
| **CO2** | 3 | - | - | 2 | 1 | 1 |
| **CO3** | 3 | 2 | 2 | 1 | - | 1 |
| **CO4** | 3 | 2 | 2 | 2 | 2 | 1 |
| **CO5** | 3 | 2 | 1 | 1 | 1 | - |

3: High, 2: Moderate, 1: Low, 0/-: No Mapping

# D Y Patil College of Engineering, Akurdi, Pune

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## FY M Tech VLSI and Embedded Systems, Semester I

**Category: Program Elective Course 1**

**Course Code: VES2409L04** **Course Title: ASIC Design**

| Teaching Scheme | | | | Evaluation Scheme | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| L | T | P | Cr | Exam | Theory % Marks | | | Practical % Marks | |
| | | | | | Max | Min for Pass | | Max | Min for Pass |
| 3 | 1 | 0 | 4 | CCA | 50 | 40 | 40 | | |
| 39 | 13 | 0 | Total:52 | ESE | 50 | 40 | | | |

**Prerequisites:** Basics of FPGA, CPLD and ASIC

**Course Objectives:**

1. To gain knowledge of the process of designing application specific algorithm for ASIC
2. To synthesize designs in EDA tool environment
3. To learn design methodologies, simulation and verification
4. To learn issues in Mixed signal ASIC design

**Course Outcomes:** After successful completion of the course the student will be able to:

| | |
|---|---|
| CO1 | Analyze the concepts and techniques of ASIC modeling. |
| CO2 | Make use of EDA tool for ASIC Simulation and Synthesis of HDL based logic Design. |
| CO3 | Interpret the algorithms used for ASIC design. |
| CO4 | Evaluate ASIC static timing analysis, delay estimation and synchronization. |
| CO5 | Construct ASIC verification and testing techniques. |

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## FY M Tech VLSI and Embedded Systems, Semester I

## Syllabus

| | | |
|---|---|---|
| **Unit I** | **Title: ASIC Modeling** | **7 hrs** |
| ASIC Modeling: IC Design Technologies, Types of ASIC and Comparisons, ASIC Design Flow, Programmable ASICs - Antifuse, SRAM, EPROM, EEPROM based ASICs. Programmable ASIC logic cells, I/O cells and programmable interconnects | | |
| **Unit II** | **Title: ASIC Simulation and Synthesis** | **8 hrs** |
| Logic Synthesis, Simulation, EDA Tools, HDL Based logic Design and Test bench, library, logic level optimization. | | |
| **Unit III** | **Title: ASIC Physical Design** | **8 hrs** |
| ASIC Physical Design: System Specifications, Architecture Design, Logic and Circuit Design, Physical Design, CAD Tools, System partitioning, Estimating ASIC Size, Power Dissipation, Partitioning Strategies, Floor planning, Area-Routing Algorithms, Placement and Routing Algorithms, Design Reuse. | | |
| **Unit IV** | **Title: ASIC Timing Analysis** | **8 hrs** |
| ASIC Timing Analysis: Static timing analysis, Timing constraints, false path detection, Timing optimization, ASIC library design, Delay estimation, mixed mode design and simulation, SI issues. | | |
| **Unit V** | **Title: ASIC Verification and Testing** | **8 hrs** |
| ASIC Verification and Testing: Different Chip Test Methods, Fault Models, Scan Test, Partial Test, Digital scan standards, BIST architecture, Memory Testing, BILBO, Boundary Scan, Self Test, JTAG, ATPG, Mixed Signal ASIC Design | | |
| **Reference Books** | | |
| 1 Smith Michael, ―Application Specific Integrated Circuits‖ Pearson Education.<br>2 Soin R S, Maloberti F, Franca J, ―Analogue-digital ASICs: circuit techniques, design tools and applications‖, IEE Publications.<br>3 Singh Raminderpal, ―Signal Integrity Effects in Custom IC and ASIC Designs‖, Wiley Publications. | | |

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## FY M Tech VLSI and Embedded Systems, Semester I

**Tutorial**

| | | |
|---|---|---|
| **Unit I** | **Title: ASIC Modeling** | **2 hrs** |
| 1. Classify Gate Array based ASICs, State types of Masked Gate Array (MGA) ASICs.<br>2. Compare different programmable ASIC technologies. | | |
| **Unit II** | **Title: ASIC Simulation and Synthesis** | **3 hrs** |
| 1. Elaborate VHDL code and test-bench code for D-flip-flop, 4-bit shift register.<br>2. Analyze logic level optimization. | | |
| **Unit III** | **Title: ASIC Physical Design** | **2 hrs** |
| 1. Demonstrate CAD tools used in ASIC Design with features.<br>2. Elaborate in brief system partitioning, floor planning and routing Algorithms/techniques in ASIC.<br>3. Differentiate floorplanning and placement in ASIC design. Differentiate global routing and detailed routing. | | |
| **Unit IV** | **Title: ASIC Timing Analysis** | **3 hrs** |
| 1. Identify one example to describe time optimization technique.<br>2. Demonstrate delays in ASIC Design. How false path detection is carried out in application specific integrated circuits. | | |
| **Unit V** | **Title: ASIC Verification and Testing** | **3 hrs** |
| 1. Draw and explain linear feedback shift register and the boundary Scanning mechanism in detail.<br>2. Explain basic automatic test pattern generator (ATPG) algorithm for A`B+ BC.<br>3. Differentiate Scan test Vs Partial test. Write short note on memory testing.<br>4. Write short note on IEEE standards 1149.1 (Joint Test Action Group). Draw daisy chained JTAG pin diagram and Write the electrical characteristics of the same.<br>5. Explain design challenges in mixed signal ASIC Design and Describe with one example gate level mixed mode simulation. | | |

# D Y Patil College of Engineering, Akurdi, Pune

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester I

### Rubrics for Continuous Evaluation

| Component | Level | Unit 1 | Unit 2 | Unit 3 | Unit 4 | Unit 5 | Total | Process Evaluation |
|---|---|---|---|---|---|---|---|---|
| Continuous Comprehensive Assessment (CCA) | Faculty | 10 | 10 | 10 | 10 | 10 | 50 | Refer CCA Guideline |
| End Semester Examination (ESE) | Institute | 10 | 10 | 10 | 10 | 10 | 50 | Each Unit Carries 10 marks Question |

### CO-PO Mapping

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 3 | 2 | 3 | 2 | 1 | 1 |
| **CO2** | 3 | - | - | 2 | 1 | 1 |
| **CO3** | 3 | 2 | 2 | 1 | - | 1 |
| **CO4** | 3 | 2 | 2 | 2 | 2 | 1 |
| **CO5** | 3 | 2 | 1 | 1 | 1 | - |

3: High, 2: Moderate, 1: Low, 0/-: No Mapping

# D Y Patil College of Engineering, Akurdi, Pune

An Autonomous Institute from AY 2024-25, Affiliated to Savitribai Phule Pune University, Pune

**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester I

**Category: Program Elective Course 1**

**Course Code: VES2409L05** **Course Title: Nanotechnology**

| Teaching Scheme | | | | Evaluation Scheme | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| L | T | P | Cr | Exam | Theory % Marks | | | Practical % Marks | |
| | | | | | Max | Min for Pass | | Max | Min for Pass |
| 3 | 1 | 0 | 4 | CCA | 50 | 40 | 40 | | |
| 39 | 13 | 0 | Total:52 | ESE | 50 | 40 | | | |

**Prerequisites:** Basics of CMOS, BiCMOS technology, FinFET technology

**Course Objectives:**

1. To get familiar with fundamental science behind Nanotechnology and systems
2. To acquire basic understanding of material science for designing NEMS based systems
3. To understand the principle of biomaterial and their applications to Bio-medical systems

**Course Outcomes:** After successful completion of the course the student will be able to:

| | |
|---|---|
| CO1 | Use quantum mechanics & quantum ideas to describe nano-structures and sensors. |
| CO2 | Choose suitable material based on the properties for Nanotechnology to learn techniques of nano-structures like CNT, nano wires. |
| CO3 | Discuss the nano-fabrication using Stamping Techniques for various applications like for Solar cell structures and Gain knowledge of designing and developing NEMS based systems. |
| CO4 | Interpret visualization and measurement of nanostructures using Nanostructure devices |
| CO5 | Characterize the principle and working of Nanolithography and it's Biomedical applications. |

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester I

## Syllabus

| | | |
|---|---|---|
| **Unit I** | **Title: Introduction to Nanotechnology** | **7 hrs** |
| The fundamental science behind nanotechnology, bio systems, molecular recognition, quantum mechanics & quantum ideas, optics. Smart materials & Sensors, self-healing structures, heterogeneous nano-structures & composites, encapsulations, natural nano-scale sensors, electromagnetic sensors, biosensors, electronic noses. | | |
| **Unit II** | **Title: Nanostructures** | **8 hrs** |
| Nanostructures, Micro/Nano-devices, nano-materials Synthesis and Applications, Molecule-Based Devices- Introduction to Carbon nanotubes.- nano-wires | | |
| **Unit III** | **Title: Micro/Nanofabrication and MEMS/NEMS** | **8 hrs** |
| Introduction to Micro/Nanofabrication- Stamping Techniques. Methods and Applications.<br>Materials Aspects of Micro- and Nano Electromechanical Systems- MEMS/NEMS , Devices and Applications. | | |
| **Unit IV** | **Title: Nanostructure Devices** | **8 hrs** |
| Nanostructure devices –Resonant tunneling diodes, Field-effect transistors, Single-electrode transfer devices. Scanning Probe Microscopy, Noncontact Atomic Force Microscopy. | | |
| **Unit V** | **Title: Nanolithography and Applications** | **8 hrs** |
| Low Temperature Scanning Probe Microscopy, Dynamic Force Microscopy.-. Nanolithography, Lithography using photons, electron beams, soft lithography. Biomedical applications. | | |
| **Reference Books** | | |
| 1. Springer Handbook of Nanotechnology<br>2. RattnerMark ,Rattner Daniel, ―Nanotechnology: A Gentle Introduction to the Next Big Idea‖<br>3. Kulkarni Sulabha K, ― Nanotechnology :Principles& Practices‖, Capital Publications<br>4. VlaimirMitin, ― Introduction to nanoelectronics science, Nanotechnology, Engineering and Applications‖, Cambridge University Press | | |

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester I

**Tutorial**

| | | |
|---|---|---|
| **Unit I** | **Title: Introduction to Nanotechnology** | **3 hrs** |
| 1. Discuss the rationale behind the evolution of Nanotechnology. | | |
| **Unit II** | **Title: Nanostructures** | **2 hrs** |
| 1. Explain various characteristics of carbon nanotubes and their applications in detail. | | |
| **Unit III** | **Title: Micro/Nanofabrication and MEMS/NEMS** | **3 hrs** |
| 1. Develop Stamping Techniques Methods and Applications.<br>2. Elaborate Micro- and Nano Electromechanical Systems- MEMS/NEMS andApplications. | | |
| **Unit IV** | **Title: Nanostructure Devices** | **3 hrs** |
| 1. Analyze the recent trends in Resonant tunneling diodes, Field-effect transistors, Single-electrode transfer devices. | | |
| **Unit V** | **Title: Nanolithography and Applications** | **2 hrs** |
| 1. Compare Low Temperature Scanning Probe Microscopy with Dynamic Force Microscopy. | | |

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester I

### Rubrics for Continuous Evaluation

| Component | Level | Unit 1 | Unit 2 | Unit 3 | Unit 4 | Unit 5 | Total | Process Evaluation |
|---|---|---|---|---|---|---|---|---|
| Continuous Comprehensive Assessment (CCA) | Faculty | 10 | 10 | 10 | 10 | 10 | 50 | Refer CCA Guideline |
| End Semester Examination (ESE) | Institute | 10 | 10 | 10 | 10 | 10 | 50 | Each Unit Carries 10 marks Question |

### CO-PO Mapping

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 3 | 2 | 3 | 2 | 1 | 1 |
| **CO2** | 3 | - | 1 | 2 | 1 | 1 |
| **CO3** | 3 | 3 | 2 | 2 | - | 1 |
| **CO4** | 3 | 2 | 2 | 2 | 2 | 1 |
| **CO5** | 3 | 2 | 1 | 1 | 1 | - |

3: High, 2: Moderate, 1: Low, 0/-: No Mapping

# D Y Patil College of Engineering, Akurdi, Pune

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester I

**Category: Program Elective Course 1**

**Course Code: VES2409L06** **Course Title: Processor Design**

| Teaching Scheme | | | | Evaluation Scheme | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| L | T | P | Cr | Exam | Theory % Marks | | | Practical % Marks | |
| | | | | | Max | Min for Pass | | Max | Min for Pass |
| 3 | 1 | 0 | 4 | CCA | 50 | 40 | 40 | | |
| 39 | 13 | 0 | Total:52 | ESE | 50 | 40 | | | |

**Prerequisites:** Computer Fundamentals, Microprocessor, VLSI Design and Technology

**Course Objectives:**

1. To learn architecture fundamentals of processor design
2. To understand memory management of CISC and RISC processors
3. To gain knowledge of architecture and design issues in DSP
4. To update the information with respect to run time reconfigurable processors

**Course Outcomes:** After successful completion of the course the student will be able to:

| | |
|---|---|
| CO1 | Apply knowledge to Visualize probable Problems, fallacies and Pitfalls in Processor Design. |
| CO2 | Make use of intermediate ISAs to allow a simple machine to emulate better pipelining approach. |
| CO3 | Design and Understand Extreme CISC and RISC, Very Long Instruction Word (VLIW), overly aggressive pipelining, unbalanced processor. |
| CO4 | Analyze and Learn DSP processor and customizable processor for SoC design. |
| CO5 | Design and Relate the run time performance parameters in reconfigurable processors for IC design and Gain skills to design and develop Asynchronous Processor design. |

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester I

## Syllabus

| | | |
|---|---|---|
| **Unit I** | **Title: Embedded Computer Architecture** | **7 hrs** |
| Embedded Computer Architecture Part-I: Components of an embedded computer, Architecture organization, ways of parallelism, I/O operations and peripherals. Problems, Fallacies, and Pitfalls in Processor Design for a high level computer instruction set architecture to support a specific language or language domain. | | |
| **Unit II** | **Title: Instruction Set Architecture** | **8 hrs** |
| Use of intermediate ISAs to allow a simple machine to emulate its betters, stack machines, overly aggressive pipelining, unbalanced processor design, Omitting pipeline interlocks,Non-power-of-2 data-word widths for general-purpose computing. | | |
| **Unit III** | **Title: Memory and Processor Design Flow** | **8 hrs** |
| Memory: Organization, Memory mapping and segmentation, Multithreading, Symmetric multiprocessing. Processor Design Flow: Capturing requirements, Instruction coding, Exploration of architecture organizations, hardware and software development. Extreme CISC and extreme RISC, Very long instruction word (VLIW). | | |
| **Unit IV** | **Title: Digital Signal Processor and Customizable processors** | **8 hrs** |
| Digital Signal Processor: Digital signal processor and its design issues, evolving architecture of DSP, next generation DSP. Customizable processors: Customizable processors and processor customization, A benefit analysis of processor customization, use of microprocessor cores in SOC design, benefits of microprocessor extensibility. | | |
| **Unit V** | **Title: Run time Reconfigurable and Asynchronous Processors** | **8 hrs** |
| Run time Reconfigurable Processors: Run time Reconfigurable Processors, embedded microprocessor trends, instruction set metamorphosis; reconfigurable computing, run-time reconfigurable instruction set processors, coarse grain reconfigurable processors. Processor Clock Generation and Distribution: Clock parameters and trends, Clock distribution networks, de-skew circuits, jitter reduction techniques, low power clock distribution, need of Asynchronous Processor Design and development | | |
| **References/Reference Books** | | |
| 1 Nurmi Jari, ―Processor Design-System on Chip Computing for ASIC‟s and FPGA‖, Springer Publications.<br>2 Frantz G, ―The DSP and Its Impact on Technology‖. | | |

3 Leibson S, Tensilica, ―Customizable Processors and Processor Customization‖.
4 Campi F, ―Run-Time Reconfigurable Processors‖.
5 Garside J, Furber S, ―Asynchronous and Self-Timed Processor Design‖.
6 Rusu S, ―Processor Clock Generation and Distribution‖.
**7** Dehon Andre, ―Reconfigurable Architecture for General purpose Computing‖.


**Tutorial**

| | | |
|---|---|---|
| **Unit I** | **Title: Embedded Computer Architecture** | **2 hrs** |
| 1. Design and relate Embedded Computer Architecture and explain with one real time example.<br>2. Design Pitfalls in Processor for a high level computer instruction set architecture to support a specific language. | | |
| **Unit II** | **Title: Instruction Set Architecture** | **3 hrs** |
| 1. Design processor for aggressive pipelining and relate it with general purpose computing.<br>2. Relate use of ISA in a simple machine with one example. | | |
| **Unit III** | **Title: Memory and Processor Design Flow** | **2 hrs** |
| 1. Relate processor with memory segmentation, multithreading and design rules with example<br>2. Relate and explore processor architecture organization with Extreme CISC, RISC and VLIW | | |
| **Unit IV** | **Title: Digital Signal Processor and Customizable processors** | **3 hrs** |
| 1. Demonstrate design issues of Digital Signal Processor with any one example.<br>2. Analyze and relate processor customization and its use. | | |

## FY M Tech VLSI and Embedded Systems, Semester I

| | | |
|---|---|---|
| **Unit V** | **Title: Run time Reconfigurable and Asynchronous Processors** | **3 hrs** |

1. Design and create clock generation and distribution systems and demonstrate.
2. Evaluate and relate run time reconfigurable processors give examples.
3. Case study and detailed explanation of Asynchronous Processor and its applications.

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester I

### Rubrics for Continuous Evaluation

| Component | Level | Unit 1 | Unit 2 | Unit 3 | Unit 4 | Unit 5 | Total | Process Evaluation |
|---|---|---|---|---|---|---|---|---|
| Continuous Comprehensive Assessment (CCA) | Faculty | 10 | 10 | 10 | 10 | 10 | 50 | Refer CCA Guideline |
| End Semester Examination (ESE) | Institute | 10 | 10 | 10 | 10 | 10 | 50 | Each Unit Carries 10 marks Question |

### CO-PO Mapping

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 3 | 2 | 3 | 2 | 1 | 2 |
| **CO2** | 3 | - | - | 2 | 1 | 1 |
| **CO3** | 3 | 2 | 2 | 2 | - | - |
| **CO4** | 3 | 2 | 2 | 3 | 2 | 1 |
| **CO5** | 3 | 2 | 1 | 2 | 1 | |

3: High, 2: Moderate, 1: Low, 0/-: No Mapping

# D Y Patil College of Engineering, Akurdi, Pune

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester I

**Category: Program Elective Course 1**

**Course Code: VES2409L07 Course Title: Wireless Sensor Networks**

| Teaching Scheme | | | | Evaluation Scheme | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| L | T | P | Cr | Exam | Theory % Marks | | | Practical % Marks | |
| | | | | | Max | Min for Pass | | Max | Min for Pass |
| 3 | 1 | 0 | 4 | CCA | 50 | 40 | 40 | | |
| 39 | 13 | 0 | Total:52 | ESE | 50 | 40 | | | |

**Prerequisites:** Basic concepts of Wireless Sensor Networks

**Course Objectives:**

1. To understand basic WSN Technology and its supporting Protocols
2. To learn routing protocols and their design issues in WSN
3. To understand sensor- management, sensor- network middleware and operating systems
4. To understand WSN layers' issues and their protocols

**Course Outcomes:** After successful completion of the course the student will be able to:

| | |
|---|---|
| CO1 | Analyze various types of WSN network and its Challenges and Constraints |
| CO2 | Examine the various types of WSN node architectures |
| CO3 | Judge different techniques of power management |
| CO4 | Analyze various attacks of Network security and it's protocol mechanism with standards and routing techniques |
| CO5 | Exhibit the knowledge of operating systems in WSN systems |

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester I

## Syllabus

| | | |
|---|---|---|
| **Unit I** | **Title: Introduction to WSN** | **7 hrs** |
| Introduction: Motivation for a Network of Wireless Sensor Nodes, Sensing and Sensors Wireless Networks, Challenges and Constraints. Applications to: Health care, Agriculture, Traffic and others. | | |
| **Unit II** | **Title: WSN Architectures** | **8 hrs** |
| Architectures: Node Architecture; the sensing subsystem, processor subsystem, communication interface, LMote, XYZ, Hogthrob node architectures. | | |
| **Unit III** | **Title: WSN performance parameter Management** | **8 hrs** |
| Power Management - Through local power, processor, communication subsystems and other means, time Synchronization needs, challenges and solutions overview for ranging techniques. | | |
| **Unit IV** | **Title: WSN security aspects and Protocols** | **8 hrs** |
| Security Fundamentals, challenges and attacks of Network Security, protocol mechanisms for security. Physical Layer- Basic Components, Source Encoding, Channel Encoding, Modulation, Signal Propagation. Medium Access Control –types, protocols, standards and characteristics, challenges Network Layer -Routing Metrics, different routing techniques. | | |
| **Unit V** | **Title: Operating Systems** | **8 hrs** |
| Operating Systems -Functional and nonfunctional Aspects, short overview of prototypes– Tiny OS, SOS, Contiki, LiteOS, Sensor grid. | | |
| **Reference Books** | | |
| 1. Dargie W., Poellabauer C., "Fundamentals of wireless sensor networks: theory and practice", John Wiley and Sons<br>2. Sohraby K., Minol, D., Znati T., "Wireless sensor networks: technology, protocols, and applications‖, John Wiley and Sons<br>3. Hart J. K.,Martinez K., ―Environmental Sensor Networks: A revolution in the earth system science‖, Earth-Science Reviews.<br>4. Feng Zhao, Leonidas J.Guibas,―Wireless Sensor Networks: An Information Processing Approach‖. | | |

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester I

**Tutorial**

| | | |
|---|---|---|
| **Unit I** | **Title: Introduction to WSN** | **2 hrs** |
| 1. Analyze various types of WSN network and discuss the Challenges and Constraints for the same. | | |
| **Unit II** | **Title: WSN Architectures** | **2 hrs** |
| 1. Examine the various types of WSN node architectures and explain in detail sensing subsystem, processor subsystem, communication interface. | | |
| **Unit III** | **Title: WSN performance parameter Management** | **3 hrs** |
| 1. Identify various power management techniques and also explain challenges and solutions overview for ranging techniques. | | |
| **Unit IV** | **Title: WSN security aspects and Protocols** | **3 hrs** |
| 1. Elaborate the challenges and attacks of Network Security and also discuss in detail thechallenges and solutions overview for ranging techniques.<br>2. Analyze the physical and Network layer in detail. | | |
| **Unit V** | **Title: Operating Systems** | **3 hrs** |
| 1. Examine the different operating systems in WSN systems and comment on Functional and nonfunctional Aspects of OS. | | |

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## FY M Tech VLSI and Embedded Systems, Semester I

## Rubrics for Continuous Evaluation

| Component | Level | Unit 1 | Unit 2 | Unit 3 | Unit 4 | Unit 5 | Total | Process Evaluation |
|---|---|---|---|---|---|---|---|---|
| Continuous Comprehensive Assessment (CCA) | Faculty | 10 | 10 | 10 | 10 | 10 | 50 | Refer CCA Guideline |
| End Semester Examination (ESE) | Institute | 10 | 10 | 10 | 10 | 10 | 50 | Each Unit Carries 10 marks Question |

## CO-PO Mapping

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 3 | 2 | 3 | 2 | 1 | 2 |
| **CO2** | 3 | - | - | 2 | 1 | 1 |
| **CO3** | 3 | 2 | 2 | 2 | - | - |
| **CO4** | 3 | 2 | 2 | 3 | 2 | 1 |
| **CO5** | 3 | 2 | 1 | 2 | 1 | |

3: High, 2: Moderate, 1: Low, 0/-: No Mapping

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester I

**Category: Program Elective Course 1**

**Course Code: VES2409L08** **Course Title: Industrial IOT in Embedded system**

| Teaching Scheme | | | | Evaluation Scheme | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| L | T | P | Cr | Exam | Theory % Marks | | | Practical % Marks | |
| | | | | | Max | Min for Pass | | Max | Min for Pass |
| 3 | 1 | 0 | 4 | CCA | 50 | 40 | 40 | | |
| 39 | 13 | 0 | Total:52 | ESE | 50 | 40 | | | |

**Prerequisites:** Basics of IoT

**Course Objectives:**

1. To understand fundamentals of IoT and embedded systems including essence, basic design strategy and process modeling.
2. To introduce students to a set of advanced topics in embedded IoT and lead them to understand research in networks.
3. To develop a comprehensive approach towards building small low cost embedded IoT systems.
4. To understand fundamentals of security in IoT.
5. To learn to implement secure infrastructure for IoT.
6. To learn real world application scenarios of IoT along with its societal and economic impact using case studies

**Course Outcomes:** After successful completion of the course the student will be able to:

| | |
|---|---|
| CO1 | Analyze IoT in Embedded system and justify various things of IoT, issues and challenges in it. |
| CO2 | Design and Implement an architecture of IoT for specified requirement |
| CO3 | Analyze various IoT protocols and it's standards and Evaluate various IoT security aspects and its challenges. |
| CO4 | Relate and Solve the given societal challenge using IoT case studies. |
| CO5 | Choose and apply between available technologies and devices for stated IoT challenge |

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## FY M Tech VLSI and Embedded Systems, Semester I

## Syllabus

| | | |
|---|---|---|
| **Unit I** | **Title: Introduction to IoT in Embedded System** | **7 hrs** |
| Introduction to Embedded System and Internet of Things o Embedded Systems, IoT: Definition and characteristics of IoT, Internet of Things: Vision, Emerging Trends, Economic Significance, Technical Building Blocks, Physical design of IoT, Things of IoT, IoT Protocols, IoT Issues and Challenges, Applications | | |
| **Unit II** | **Title: Embedded IoT Platform** | **8 hrs** |
| Embedded IoT Platform Design Methodology Purpose and requirement specification, Process specification, Domain model specification, information model specification, Service specifications, IoT level specification, Functional view specification, Operational view specification, Device and component integration, Application development | | |
| **Unit III** | **Title: IoT Protocols and security** | **8 hrs** |
| IoT Protocols: Protocol Standardization for IoT, M2M and WSN Protocols, SCADA and RFID Protocols, Issues with IoT Standardization, Unified Data Standards, Protocols – IEEE 802.15.4, BACNet Protocol, Modbus, KNX, Zigbee Architecture, Network layer, APS layer. IoT Security: Vulnerabilities of IoT, Security Requirements, Challenges for Secure IoT, Threat Modeling, Key elements of IoT Security: Identity establishment, Access control, Data and message security, Non-repudiation and availability, Security model for IoT | | |
| **Unit IV** | **Title: IoT Case Studies** | **8 hrs** |
| IoT Physical Servers, Cloud Offerings and IoT Case Studies: Introduction to Cloud Storage Models, Communication API, WAMP: Autobahn for IoT | | |
| **Unit V** | **Title: IoT Case Studies based on Cloud and Web technology** | **8 hrs** |
| Xively Cloud for IoT, Python Web Application Framework: Django, Amazon Web Services for IoT, Skynet IoT Messaging Platform. Case Studies: Home Intrusion Detection, Weather Monitoring System, Air Pollution Monitoring, Smart Irrigation | | |
| **Text Books** | | |
| 1. HakimaChaouchi, ― The Internet of Things Connecting Objects to the Web‖ISBN : 978-1-84821-140-7, Wiley Publications<br>2. Olivier Hersent, David Boswarthick, and Omar Elloumi, ―The Internet of Things: Key | | |

## FY M Tech VLSI and Embedded Systems, Semester I

| **Reference Books** |
|---|
| 1. Vijay Madisetti, Arshdeep Bahga, ―Internet of Things: A Hands-On Approach‖<br>2. Waltenegus Dargie, Christian Poellabauer, "Fundamentals of Wireless Sensor Networks: Theory and Practice"<br>3. Daniel Minoli, ―Building the Internet of Things with IPv6 and MIPv6: The Evolving World of M2M Communications‖, ISBN: 978-1-118-47347-4, Wiley Publications<br>4. Pethuru Raj and Anupama C. Raman, "The Internet of Things: Enabling Technologies,Platforms, and Use Cases", CRC Press |

**Tutorial**

| | | |
|---|---|---|
| **Unit I** | **Title: Introduction to IoT in Embedded System** | **2 hrs** |
| 1. Design Embedded system using Industrial IoT<br>2. Relate various industrial IoT issues and challenges for various applications. | | |
| **Unit II** | **Title: Embedded IoT Platform** | **2 hrs** |
| 1. Design and analyze Embedded IoT platform for specific requirements.<br>2. Explore functional view, operational view of Embedded IoT platform with one example | | |
| **Unit III** | **Title: IoT Protocols and security** | **3 hrs** |
| 1. Relate and express significance of various IoT protocols.<br>2. Demonstrate M2M and WSN protocols with any real time example.<br>3. Design IoT security System by considering various challenges in security requirements of IoT systems.<br>4. Demonstrate any security model for Industrial IoT. | | |
| **Unit IV** | **Title: IoT Case Studies** | **3 hrs** |
| 1. Case studies of IoT physical servers, cloud offerings. | | |

| | | |
|---|---|---|
| **2.** Analysis and presentation of Case studies of Cloud storage model and WAMP: Autobahn for IoT. | | |
| **Unit V** | **Title: IoT Case Studies based on Cloud and Web Technology** | **3 hrs** |
| 1. Detailed Advance Case study for various applications of Industrial IoT. | | |

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## FY M Tech VLSI and Embedded Systems, Semester I

## Rubrics for Continuous Evaluation

| Component | Level | Unit 1 | Unit 2 | Unit 3 | Unit 4 | Unit 5 | Total | Process Evaluation |
|---|---|---|---|---|---|---|---|---|
| Continuous Comprehensive Assessment (CCA) | Faculty | 10 | 10 | 10 | 10 | 10 | 50 | Refer CCA Guideline |
| End Semester Examination (ESE) | Institute | 10 | 10 | 10 | 10 | 10 | 50 | Each Unit Carries 10 marks Question |

## CO-PO Mapping

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 3 | 2 | 3 | 2 | 1 | 2 |
| **CO2** | 3 | - | - | 2 | 1 | 1 |
| **CO3** | 3 | 2 | 2 | 2 | - | - |
| **CO4** | 3 | 2 | 2 | 3 | 2 | 1 |
| **CO5** | 3 | 2 | 1 | 2 | 1 | |

3: High, 2: Moderate, 1: Low, 0/-: No Mapping

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An Autonomous Institute from AY 2024-25, Affiliated to Savitribai Phule Pune University, Pune

**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester I

**Category: Program Core Laboratory**

**Course Code: VES2409P01 Course Title: Laboratory Practice I**

| Teaching Scheme | | | | Evaluation Scheme | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| L | T | P | Cr | Exam | Theory % Marks | | Practical % Marks | | |
| | | | | | Max | Min for Pass | Max | Min for Pass | |
| 0 | 0 | 4 | 2 | CCA | -- | -- | 50 | 20 | 40 |
| 0 | 0 | 52 | Total: 52 | ESE | -- | -- | 50 | 20 | |

**Prerequisites:**

1. Front End Tools and Back End Tools basics
2. C Language basics and Interfacing basics

**Course Objectives:**

1. To understand the significance of CMOS design in VLSI
2. To learn Hardware and Software design tools
3. To design Embedded Systems for real time application
4. To learn ARM 7 architecture and its programming concepts

**Course Outcomes:** After successful completion of the course the student will be able to:

| | |
|---|---|
| CO1 | Design digital logic circuits using CMOS technology. |
| CO2 | Interface the advanced peripherals to ARM based microcontrollers. |
| CO3 | Design and analyze various performance parameters of circuits with HDL code, Embedded programming in C and Keil etc. usingfront end tool and draw layout of digital/analog circuits using back end tool. |
| CO4 | Apply DRC's of appropriate foundry, draw the layout and simulate different digital/analog circuits using backend tool like Microwind, Mentorgraphics, Cadence etc. |
| CO5 | Implement, design and simulate various nanostructures, processors internal functional blocks like CPU and Embedded system on PLD or IoT platform. |

# D Y Patil College of Engineering, Akurdi, Pune

An Autonomous Institute from AY 2024-25, Affiliated to Savitribai Phule Pune University, Pune

**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester I

| **Syllabus** | | |
|---|---|---|
| | **Introduction** | **06 hrs** |
| Laboratory Practice I (LP I) is companion course of theory courses (core and elective) in Semester I. It is recommended that set of assignments or at least one study project per course is to be completed. Set of problem statements are suggested. Course/ Laboratory instructor may frame suitable problem statements. Student has to submit a report/Journal consisting of appropriate documents -prologue, Certificate, table of contents, and other suitable write up like (Introduction, motivation, aim and objectives, outcomes, brief theory, requirements analysis, design aspects, algorithms, mathematical model, complexity analysis, results, analysis and conclusions). | | |
| | **Guidelines for CCA** | **05 hrs** |
| Continuous assessment of laboratory work is done based on performance of student.<br>Each assignment/ mini project assessment is to be done based on parameters with appropriate weightage. Suggested parameters for overall assessment as well as mini project assessment include-timely completion, performance, innovation, efficient codes, usability, documentation and adhering to SDLC comprehensively | | |
| | **Guidelines for ESE** | **05 hrs** |
| It is recommended that examination should be conducted as presentation by student based on one of the mini projects completed and the content understanding of laboratory work. | | |
| | **Lab practice file shall consist of following assignments/experiments** | |
| **Guidelines:**<br>1. Total experiments to be conducted are two from each Part: Part A to Part D<br>2. Total: 08 experiments | | |
| **Detailed Syllabus:** | | |
| | **Part A: Digital CMOS Design** | **9 hrs** |
| **Expt. No.** | **Title** | |
| 1. | To design, prepare layout and simulate CMOS Inverter for the given specifications of load capacitance, propagation delay, power dissipation, foundry etc. | |
| 2. | To design CMOS logic for F = A + B (C + D) + EFG and prepare layout. Assume suitable capacitive load & foundry. Measure TR, TF & TPD. | |
| 3. | To draw FSM diagrams, write HDL code, synthesize, simulate, place & route for a Tea/Coffee vending machine. Generalized I/Os of the machine are coin sense, cup sense, option sense, pour valve, timer count, alarm etc. You may assume additional I/Os too. | |
| 4. | Design and simulate adder/multiplexer/decoders using CMOS and Transmission Gate. | |
| **Part B: Embedded System Design** | | **9 hrs** |
| 1. | Write a program for 4*4 Matrix Keypad Interface. | |
| 2. | Interfacing EEPROM to LPC2148 using I2C protocol | |

| | |
|---|---|
| 3. | Interfacing USB & CAN of LPC 1768. |
| 4. | One experiment based on any one development Platform: Arduino, Beaglebone, Raspberry Pi, Intel Galileo Gen 2. |
| **Part C: Reconfigurable Computing** | **9 hrs** |
| 1. | Execute the Xilinx ISE tool design flow and verify for various modeling styles of VHDL with suitable examples on FPGA. |
| 2. | To design and implement a Multi Context (4) 4-LUT and implement using HDL and download on FPGA. |
| 3. | Implement top level modular and hierarchical designs of Adder and Subtractor such that they can be replaced. |
| 4. | Implement an adaptive design of LED shifter (Right & Left shift) |
| **Part D: Program Elective course experiments** | **9 hrs** |
| **ASIC Design** | |
| 1. | Write HDL code to simulate, synthesis, place & route FIFO on PLD. Check results and also write the test bench. |
| 2. | Draw CMOS layout & simulate shift register by applying DRC's of appropriate foundry using backend tool and check the output |
| 3. | Draw CMOS layout & simulate 16:1 MUX by applying DRC's of appropriate foundry using backend tool and check the output. |
| 4. | Simulate Stuck at fault model of given function. |
| **Nano Technology** | |
| 1. | Introduction of analysis and characterization of Nano structured materials, coating and thin film sensors. |
| 2. | Surface tension measurement of Nano fluids. |
| 3. | To observe size and slope of the Nano sized sample using scanning electron microscopy. |
| 4. | Design, simulation and analysis of Nano structures. |
| **Processor Design** | |
| 1. | Design and implement MAC module on PLD |
| 2. | Design and implement CPU on PLD |
| 3. | Design and implement Carry look-ahead generator on PLD |

| | |
|---|---|
| 4. | Design and implementation of Translation look-aside buffer. |
| **Wireless Sensor Networks** | |
| 1. | Reading data from Sensor node. |
| 2. | Implement 50 stationary nodes topology using NS2 for data transmission and record QoS parameters of the Networks/ Test bed. |
| 3. | Implement 50 dynamic nodes topology using NS2 for data transmission and record |
| | QoS parameters of the Networks /Test bed. |
| 4. | On any above topology change the Network layer/Transport layer/MAC layer protocol and monitor the changes between any two protocols/ test bed using Network Simulator. |
| **Industrial IOT in Embedded system** | |
| 1. | Weather forecasting system using any cloud applications and IoT hardware platforms. |
| 2. | Smart Agriculture irrigation System. |
| 3. | Motion detection-based Intrusion detection and alert system. |
| 4. | Smart Air pollution monitoring system. |

## Rubrics for Continuous Evaluation

| **Component** | **Level** | **Laboratory Practice -I** | **Total** | **Passing** | **Process Evaluation** |
|---|---|---|---|---|---|
| Continuous Comprehensive Assessment (CCA) | Faculty | 1. Design with Advanced Engineering Materials<br>2. Mechanism Analysis and Synthesis<br>3. Advanced Mechanics of Solids | 50 | 20 | Refer CCA Guideline |
| ESE | Institute | | 50 | 20 | External Oral Exam |

# D Y Patil College of Engineering, Akurdi, Pune

An Autonomous Institute from AY 2024-25, Affiliated to Savitribai Phule Pune University, Pune

**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester I

## CO-PO Mapping

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 3 | 2 | 2 | 2 | 1 | 1 |
| **CO2** | 3 | 2 | 2 | 2 | 1 | 1 |
| **CO3** | 3 | 2 | 2 | 2 | 1 | 1 |
| **CO4** | 2 | 1 | 1 | 1 | 1 | 1 |
| **CO5** | 3 | 1 | 1 | 2 | 1 | 1 |

3: High, 2: Moderate, 1: Low, 0/-: No Mapping

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# D Y Patil College of Engineering, Akurdi, Pune

An Autonomous Institute from AY 2024-25, Affiliated to Savitribai Phule Pune University, Pune

**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester I

**Category: Research Course**

**Course Code: RMD24O9L01** **Course Title: Research Methodology**

| Teaching Scheme | | | | Evaluation Scheme | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| L | T | P | Cr | Exam | Theory % Marks | | | Practical % Marks | |
| | | | | | Max | Min for Pass | | Max | Min for Pass |
| 3 | 0 | 0 | 3 | CCA | 50 | 40 | 40 | -- | -- |
| 39 | 0 | 0 | Total: 39 | ESE | 50 | 40 | | | |

**Prerequisites**: Basic understanding of statistics like central tendency, dispersions, Basic computing skills likes Microsoft Excel, Data analysis, critical thinking skills like reasoning etc

**Course Objectives:** Purposes of Course are:

1. To Provide a comprehensive understanding of research methods, techniques, and their applications in engineering and technology.
2. To Enable students to critically analyze and synthesize literature relevant to their research field.
3. To Equip students with the skills to design and conduct scientific research effectively using appropriate methodologies.
4. To Instill ethical standards, promoting integrity accountability and responsibilities in conducting and reporting research

**Course Outcomes:** After Successful completion of course units, students will

| | |
|---|---|
| CO1 | Effectively apply research processes and methodologies relevant to engineering research, facilitating the foundation of research activities, while developing the ability to conduct a thorough literature review to critically assess existing work and identify gaps for contributing to innovative research. |
| CO2 | Design and execute a research study using quantitative and qualitative research methods to yield reliable and valid data ensuring robustness of research findings |
| CO3 | Analyze data using statistical tools and software, interpreting results accurately to make informed decisions based on research results |
| CO4 | Author research findings and present in both written and oral formats effectively to both scientific and lay audiences |
| CO5 | Appraise the ethical standards of research, acknowledging the work of others appropriately and reporting results truthfully |

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester I

| Syllabus | | |
|---|---|---|
| **Unit I** | **Basics of Research & Literature Review Techniques** | **10hrs** |
| Definition of research, research methodology, concepts and significance of research in engineering, research ethics and responsibilities**,** case studies and real-life examples**,** Sources of Scientific literature, Methods for conducting and organizing literature reviews, Tools for managing references and citations like Mendeley, case studies and real-life examples | | |
| **Unit II** | **Research Design** | **08hrs** |
| Types of research design: Experimental, Correlational, Survey and Case Study, variables, sampling methods and techniques, formulating experimental and observational strategies, case studies and real-life examples | | |
| **Unit III** | **Data Collection and Analysis** | **07hrs** |
| Techniques for collecting primary and secondary data, quantitative analysis, descriptive and inferential statistics, qualitative analysis, content and thematic analysis, case studies and real-life examples | | |
| **Unit IV** | **Statistical Tools and Software in Research** | **08hrs** |
| Usage of Statistical software's like Minitab, MATLAB/Scilab in data analysis and interpretations, visualizing data and presenting statistical results in graphical, numerical format, case studies and real-life examples | | |
| **Unit V** | **Research Reporting and Presentation** | **06 hrs** |
| Structure and components of research reports and papers, Ethical considerations in publishing, Skills for effective research presentation, case studies and real-life examples | | |

**Tutorials:**

All activities should be published in LinkedIn or YouTube and record responses.

1) Write a brief essay on the importance of research in their field of engineering

2) Create a flowchart of the research process for a hypothetical study

3) Group discussion on recent engineering innovations driven by research

4) Analyze a case study on ethical dilemmas in research and propose solutions.

5) Create a literature review by using Mendeley as per APA citations and references

6) Choose a research question and propose a suitable research design

7) Outline experimental protocol for given research question

8) Analyze a dataset using Minitab/Scilab/MATLAB and interpret the results

9) Prepare a check sheet for selection of type of graphs and its effectiveness

10) Review and critique a research paper for ethical compliance

## FY M Tech VLSI and Embedded Systems, Semester I

**References:**


1. Kothari, C. R. (2019). Research methodology: Methods and techniques. New Age International.
2. Kumar, R. (2019). Research methodology: A step by step guide for beginners. Sage Publications.
3. Kothari, C. R., & Garg, G. (2019). Research methodology: Methods and techniques. New Age International.
4. Chawla, D., & Sondhi, N. (2021). Research methodology: Concepts and cases. Vikas Publishing House.
5. Prasad, R. K. (2020). Research methodology. Kitab Mahal.
6. Tripathi, P. C. (2018). Research methodology in social science. Sarup & Sons.
7. Thomas, G. (2022). Research methodology and scientific writing. Springer.


**Research Papers:**


1. Snyder, H. (2019). Literature review as a research methodology: An overview and guidelines. In Journal of Business Research (Vol. 104, pp. 333–339). Elsevier BV. https://doi.org/10.1016/j.jbusres.2019.07.039
2. Kolstoe, S. E., Durning, J., Yost, J., & Aleksandrova-Yankulovska, S. (2023). Ranking Research Methodology by Risk — a cross-sectional study to determine the opinion of research ethics committee members. In Systematic Reviews (Vol. 12, Issue 1). Springer Science and Business Media LLC. https://doi.org/10.1186/s13643-023-02295- 1


**NPTEL/SWAYAM**

1) Research Methodology - https://www.youtube.com/watch?v=E2gGF1rburw

2) Issues in hypothesis testing part 1- https://www.youtube.com/watch?v=p2M_0e5bxTA

3) Issues in hypothesis testing part 2 - https://www.youtube.com/watch?v=KSwM5qo_yoQ

### Rubrics for Continuous Evaluation

| Component | Level | Unit 1 | Unit 2 | Unit 3 | Unit 4 | Unit 5 | Total | Process Evaluation |
|---|---|---|---|---|---|---|---|---|
| Continuous Comprehensive Assessment (CCA) | Faculty | 10 | 10 | 10 | 10 | 10 | 50 | Refer CCA Guideline |
| End Semester Examination (ESE) | Institute | 10 | 10 | 10 | 10 | 10 | 50 | Each Unit Carry 10 marks Question |

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester I
## CO-PO Mapping

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 3 | 2 | 3 | 2 | 2 | 3 |
| **CO2** | 3 | 2 | 2 | 3 | 3 | 3 |
| **CO3** | 3 | 2 | 3 | 2 | 3 | 3 |
| **CO4** | 3 | 2 | 2 | 3 | 3 | 3 |
| **CO5** | 2 | 3 | 3 | 3 | 3 | 3 |

3: High, 2: Moderate, 1: Low, 0/-: No Mapping

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# D Y Patil College of Engineering, Akurdi, Pune

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester I

**Category: Research Course**

**Course Code: VES2409P02** **Course Title: Research Seminar**

| Teaching Scheme | | | | Evaluation Scheme | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| L | T | P | Cr | Exam | Theory % Marks | | Practical % Marks | | |
| | | | | | Max | Min for Pass | Max | Min for Pass | |
| 0 | 0 | 2 | 1 | CCA | -- | -- | TW 50 | 20 | 40 |
| 0 | 0 | 26 | Total: 26 | ESE | | | OR 50 | 20 | |

**Category: Engineering Course**

A research seminar is an in-depth academic course designed to enhance student's research skills and knowledge in a specific field. It involves regular meetings where students present their research progress, engage in critical discussions, and receive feedback from peers and instructors.

**Prerequisites: Advances in Engineering & technology**

**Course Objectives:**

1. To expose students to latest advancements in advanced engineering to address real world challenges.
2. To foster skills in scientific communication and presentation through structured research findings.

**Course Outcomes:** After successful completion of the course the student will be able to

| | |
|---|---|
| CO1 | Analyse research findings and technological innovations in the advancement of engineering field |
| CO2 | Develop theoretical and practical knowledge to propose solutions to complex engineering research problems |

**Syllabus**

Task 1 Selection of broad research domain
Task 2 Literature Review
Task 3 Methodologies for research work
Task 4 Experimentation/Simulation/Numerical analysis/mathematical modelling
Task 5 Results & Discussion
Task 6 Summary
Prepare a research seminar report and present.

**References Books:**


- Booth, W. C., Colomb, G. G., Williams, J. M., Bizup, J., & FitzGerald, W. T. (2016). The craft of research (4th ed.). University of Chicago Press.
- Capstone, R. H. (2015). Designing and teaching undergraduate capstone courses. Jossey-Bass
- Limonta, C. H., Corsi, M., & White, D. J. (2020). Effective scientific communication: The other half of science. Oxford University Press.
- Day, R. A., & Gastel, B. (2016). How to write and publish a scientific paper (8th ed.). Greenwood.

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester I

### Rubrics for Continuous Evaluation

| Component | Level | Research Seminar | Total | Process Evaluation |
|---|---|---|---|---|
| Continuous Comprehensive Assessment (CCA) | Faculty | To findings and technological innovations in the advancement of engineering field and prepare a report | 50 | Refer CCA Guideline |
| ESE | Institute | Research Seminar Presentation | 50 | Oral |

### CO-PO Mapping

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 2 | 2 | 2 | 3 | 2 | 3 |
| **CO2** | 2 | 2 | 2 | 3 | 2 | 3 |

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# D Y Patil College of Engineering, Akurdi, Pune

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**Department of Electronics and Telecommunication**

**FY M Tech VLSI and Embedded Systems, Semester I**

**Category: Non Credit Course**

**Course Code: NCC2409L02-A** **Course Title: Disaster Management**

| Teaching Scheme | | | | Evaluation Scheme | | | | |
|---|---|---|---|---|---|---|---|---|
| L | T | P | Cr | Exam | Theory % Marks | | Practical % Marks | |
| | | | | | Max | Min for Pass | Max | Min for Pass |
| 2 | 0 | 0 | 0 | CCA | 100 | 40 | - | - |
| 26 | 0 | | Total: 26 | | | | | |

**Category: Engineering Course**

**Prerequisites:**

Basic Understanding of Geography and Environmental Science, Knowledge of emergency protocols, first aid, and the roles of various agencies in disaster response and recovery, Knowledge of Risk Assessment and Management.

**Course Objective:**

1. Understand disaster risk management.
2. Develop emergency response skills.
3. Enhance disaster resilience.

**Course Outcomes:** After successful completion of the course the student will be able to

| | |
|---|---|
| CO1 | Learning and understanding the basic knowledge of Disaster Management concept and different approaches to reduce the impact of disaster |
| CO2 | Understand the types of disaster their origin causes and their management and the disaster profile of India |
| CO3 | Learning to apply the knowledge of technology for monitoring and management of the disaster |
| CO4 | Drill based learning of disaster management |

**Syllabus**

| Unit I | Introduction on Disaster | 07 hrs |
|---|---|---|

Different Types of Disaster :
A) Natural Disaster: such as Flood, Cyclone, Earthquakes, Landslides etc
B) Man-made Disaster: such as Fire, Industrial Pollution, Nuclear Disaster, Biological Disasters, Accidents (Air, Sea, Rail & Road), Structural failures(Building and Bridge), War & Terrorism etc. Causes, effects and practical examples for all disasters.

| Unit II | Mitigation and Management techniques of Disaster | 07 hrs |
|---|---|---|

Basic principles of disasters management and crisis management, Disaster Management cycle, Scopes of and criteria of prevention and mitigation of disasters, Aspects of disaster response and Recovery, Important criteria of relief Mechanism.

| Unit III | Geo-informatics in Disaster Management | 06 hrs |
|---|---|---|

Remote Sensing (RS), Geographical information system (GIS), Global Positioning Service (GPS), Indian Regional Navigation Satellite System (IRNSS): NavIC Indian Tsunami Early Warning System (ITEWS) Use of ICT and mobile technology for Disaster management, Application of Drone.

| Unit IV | Disaster Management Act | 06 hrs |
|---|---|---|

Disaster Management Act 2005, Institutional framework under Disaster Management act 2005, Role of National Disaster Management Authority (NDMA) Search and Rescue Operations, (one and two-person method) Demonstration of Earthquake Evacuation Drill Demonstration of Fire Drill

## FY M Tech VLSI and Embedded Systems, Semester I

**ReferenceBooks**


1. Savindra Singh, Jeetendra Singh, Disaster management, Pravalika Publications,Allahabad,2016
2. Alexander David, Introduction in Confronting Catastrophe, Oxford University Press, 2000.
3. Kapur, Anu& others, Disasters in India Studies of grim reality, Rawat Publishers, Jaipur,2005.
4. Mukta Girdhar, Natural Disasters, Amy publication, Dariyaganj, New Delhi, 2019.
5. Dr. Mrinalini Pandey, Disaster Management, Wiley India Pvt. Ltd.
6. Andharia J. Vulnerability in Disaster Discourse, JTCDM, Tata Institute of Social SciencesWorking Paper No. 8, 2008.
7. Govt. of India: Disaster Management Act 2005, Government of India, New Delhi


**WebReferences**

1. https://onlinecourses.swayam2.ac.in/cec19_hs20/preview
2. https://nptel.ac.in/courses/124107010
3. https://archive.nptel.ac.in/courses/105/104/105104183/

### Rubrics for Continuous Evaluation

| Component | Level | Unit 1 | Unit 2 | Unit 3 | Unit 4 | Total | Passing | Process Evaluation |
|---|---|---|---|---|---|---|---|---|
| Continuous Comprehensive Assessment (CCA) | Faculty | 25 | 25 | 25 | 25 | 100 | 40 | Refer CCA Guideline |

### CO-PO Mapping

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 3 | 3 | 3 | 3 | 1 | 2 |
| **CO2** | 3 | 3 | 2 | 3 | 2 | 3 |
| **CO3** | 3 | 1 | 2 | 2 | 3 | 3 |
| **CO4** | 3 | 3 | 3 | 2 | 2 | 2 |

3: High, 2: Moderate, 1: Low, 0: No Mapping

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# D Y Patil College of Engineering, Akurdi, Pune

An Autonomous Institute from AY 2024-25, Affiliated to Savitribai Phule Pune University, Pune

**Department of Electronics and Telecommunication**

**FY M Tech VLSI and Embedded Systems, Semester I**

**Category: Non Credit Course**

**Course Code: NCC2409L02-B** **Course Title: Value Education**

| Teaching Scheme | | | | Evaluation Scheme | | | | |
|---|---|---|---|---|---|---|---|---|
| L | T | P | Cr | Exam | Theory % Marks | | Practical % Marks | |
| | | | | | Max | Min for Pass | Max | Min for Pass |
| 2 | 0 | 0 | 0 | CCA | 100 | 40 | - | - |
| 26 | 0 | | Total: 26 | | | | | |

**Category: Engineering Course**

**Prerequisites:**

Basic Understanding of Ethical Principles, Awareness of Cultural and Social Norms

**Course Objective:**

1. Cultivate an understanding of ethical principles and values, promoting integrity, honesty, and responsibility in personal and professional life.
2. Develop empathy and respect towards diverse perspectives, cultures, and beliefs, fostering inclusive and compassionate attitudes.
3. Encourage critical thinking skills to evaluate moral dilemmas and make ethical decisions aligned with personal values and societal well-being.

**Course Outcomes:** After successful completion of the course the student will be able to

| | |
|---|---|
| CO1 | Understand the meaning of values and culture |
| CO2 | Develop as social responsibility, Create a communal harmonious society and practice unity in diversity |
| CO3 | Identify the power of thoughts and words |
| CO4 | Correlate the relationship between values and human rights |

**Syllabus**

| | | |
|---|---|---|
| **Unit I** | **Introduction to Value Education** | **07 hrs** |
| Value Education – Definition, Evolution of value oriented education, Concept of Human Values – Family Values - Aesthetic Values – Ethical Values – Spiritual Values | | |
| **Unit II** | **Character Formation: Personal & Personality Development** | **07 hrs** |
| Self-Discipline – Self-Confidence – Self-Initiative – Self-awareness –Empathy – Compassion – Forgiveness – Honesty and Courage<br>Leadership qualities – Personality Development | | |
| **Unit III** | **The Power of Mind** | **06 hrs** |
| Definition, Meaning, Scope of Yoga - Aims and objectives of Yoga - Yoga Education with modern context - Different traditions and schools of Yoga - Yoga practices: Controlling Mind – Physical Exercise –Meditation – Mudras – Yoga – – Asanas<br>Concept of Mind in the Upanishads – Moralization of Desires – Neutralization of Anger – Five Ways to Check Worry Habit and Eradication – Benefits of Blessings.<br>The Power of Mind – the Power of Positive Thinking | | |
| **Unit IV** | **Human Rights and Universal Values** | **06 hrs** |
| Concept of Human Rights – Classifications of Human Rights and Relevant Constitutional | | |

## FY M Tech VLSI and Embedded Systems, Semester I

Provisions: Right to Life, liberty ad Dignity- Right to equality- Right against exploitation- Cultural and Educational Right- Economic Rights- Political Rights- Social Rights - Human Rights of Women and Children – Peace and harmony.

### ReferenceBooks

**Text Books**


1. Das, M.S. & Gupta, V.K, Social Values among Young adults: A changing Scenario, MD Publications, New Delhi, 1995

2. Vivekananda, Swami, Personality Development, Advaita Ashrama, Kolkata, 2008

3. R. C. Pradhan, Language and Mind in the Upanishads, Language and Mind: The Classical Indian Perspective, ed. K. S. Prasad, Hyderabad Studies in Philosophy no. 5, Decent Books, New Delhi, 2008

4. Vincent Peale, Norman, Six Attitudes for Winners, Jaico Publishing House, Mumbai, 2009.

5. Dr. Mrinalini Pandey, Disaster Management, Wiley India Pvt. Ltd.


**Reference Books**


1. Andharia J. Vulnerability in Disaster Discourse, JTCDM, Tata Institute of Social SciencesWorking Paper No. 8, 2008.

2. Govt. of India: Disaster Management Act 2005, Government of India, New Delhi


### WebReferences

1. https://www.hzu.edu.in/bed/Basics-in-Education%20(NCERT).pdf
2. https://nptel.ac.in/content/storage2/courses/109101003/downloads/Lecture-6.pdf
3. 3. https://nptel.ac.in/content/storage2/courses/109104115/PDF/lec38.pdf

## Rubrics for Continuous Evaluation

| Component | Level | Unit 1 | Unit 2 | Unit 3 | Unit 4 | Total | Passing | Process Evaluation |
|---|---|---|---|---|---|---|---|---|
| Continuous Comprehensive Assessment (CCA) | Faculty | 25 | 25 | 25 | 25 | 100 | 40 | Refer CCA Guideline |

## CO-PO Mapping

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 3 | 3 | 3 | 3 | 1 | 2 |
| **CO2** | 3 | 3 | 2 | 3 | 2 | 3 |
| **CO3** | 3 | 1 | 2 | 2 | 3 | 3 |
| **CO4** | 3 | 3 | 3 | 2 | 2 | 2 |

3: High, 2: Moderate, 1: Low, 0: No Mapping

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# D Y Patil College of Engineering, Akurdi, Pune

An Autonomous Institute from AY 2024-25, Affiliated to Savitribai Phule Pune University, Pune

**Department of Electronics and Telecommunication**

**FY M Tech VLSI and Embedded Systems, Semester I**

**Category: Non Credit Course**

**Course Code: NCC2409L02-C** **Course Title: Constitution of India and Indian Knowledge System**

| Teaching Scheme | | | | Evaluation Scheme | | | | |
|---|---|---|---|---|---|---|---|---|
| L | T | P | Cr | Exam | Theory % Marks | | Practical % Marks | |
| | | | | | Max | Min for Pass | Max | Min for Pass |
| 2 | 0 | 0 | 0 | CCA | 100 | 40 | - | - |
| 26 | 0 | | Total: 26 | | | | | |

**Category: Engineering Course**

**Prerequisites:**

Basic Understanding of Indian History. Basic concepts such as democracy, federalism, and the separation of powers. Awareness of contemporary political and legal issues in India. Ability to read and understand complex legal and political texts. Indian Knowledge System

**Course Objective:**

1. Explore the historical background and evolution of the Constitution of India, examining the factors and events that influenced its development.
2. Comprehensive understanding of the structure, fundamental principles, and values enshrined in the Constitution, including democracy, equality, secularism, and justice.
3. Evaluate the fundamental rights and duties of citizens, the structure and functions of central and state governments, and the significance of key constitutional provisions and amendments in shaping India's governance and society.
4. Understand the rich heritage of ancient India.

**Course Outcomes:** After successful completion of the course the student will be able to

| | |
|---|---|
| CO1 | Understand the historical context and the making of the Indian Constitution. |
| CO2 | Analyze the Preamble, fundamental rights, duties, and directive principles. |
| CO3 | Describe the structure and functions of the central and state governments and also Interpret key constitutional provisions and understand the amendment process. |
| CO4 | Appreciate the significance of major constitutional bodies and landmark judgments |

**Syllabus**

| | | |
|---|---|---|
| **Unit I** | **Introduction to the Constitution of India** | **07 hrs** |
| *Historical Background:* Making of the Indian Constitution, Constituent Assembly, influences from other constitutions.<br>*Preamble:* Philosophy, objectives, and interpretation.<br>*Salient Features:* Federal structure, parliamentary system, separation of powers, fundamental rights and duties. | | |
| **Unit II** | **Fundamental Rights and Duties** | **07 hrs** |
| *Fundamental Rights:* Equality, Freedom, Protection from exploitation, Freedom of religion, Cultural and educational rights, Constitutional remedies.<br>*Directive Principles:* Classification, significance, and relation with Fundamental Rights.<br>*Fundamental Duties:* Importance and implementation. | | |
| **Unit III** | **Structure and Functions of Governments and Constitutional Provisions and Amendments** | **06 hrs** |

## FY M Tech VLSI and Embedded Systems, Semester I

*Union Government:* President, Prime Minister and Council of Ministers, Parliament.
*State Government:* Governor, Chief Minister and Council of Ministers, State Legislature.
*Judiciary:* Supreme Court, High Courts, Subordinate Courts.
*Emergency Provisions:* Types, implications.
*Special Provisions:* For states and regions, Scheduled and Tribal Areas.
*Amendments:* Procedure, major amendments, Basic Structure Doctrine.
*Constitutional Bodies:* Election Commission, CAG, UPSC, Finance Commission.

| **Unit IV** | **Indian Knowledge System** | **06 hrs** |
|---|---|---|

IKS Domains: Vedanta, Vedic Literature, Science, Mathematics, Astronomy, Ayurveda, Yoga, Ashtang Yoga, Indian Architecture and Town Planning, Indian Fine Arts, Indian Metallurgy, Agriculture

**ReferenceBooks**


1. Introduction to the Constitution of India, by D.D. Basu
2. Indian Polity, by M. Laxmikanth
3. Our Constitution, by SubhashKashyap


**Reference Books**


1. Journals and Articles: Constitutional Law journals, law review articles.


**WebReferences**

Government of India, Ministry of Law and Justice, National Portal of India
https://iksindia.org/

## Rubrics for Continuous Evaluation

| Component | Level | Unit 1 | Unit 2 | Unit 3 | Unit 4 | Total | Passing | Process Evaluation |
|---|---|---|---|---|---|---|---|---|
| Continuous Comprehensive Assessment (CCA) | Faculty | 25 | 25 | 25 | 25 | 100 | 40 | Refer CCA Guideline |

## CO-PO Mapping

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 3 | 3 | 3 | 3 | 1 | 2 |
| **CO2** | 3 | 3 | 2 | 3 | 2 | 3 |
| **CO3** | 3 | 1 | 2 | 2 | 3 | 3 |
| **CO4** | 3 | 3 | 3 | 2 | 2 | 2 |

3: High, 2: Moderate, 1: Low, 0: No Mapping

*****

# D Y Patil College of Engineering, Akurdi, Pune

An Autonomous Institute from AY 2024-25, Affiliated to Savitribai Phule Pune University, Pune

**Department of Electronics and Telecommunication**

**FY M Tech VLSI and Embedded Systems, Semester I**

**Course Category: Non Credit Course**

**Course Title: Pedagogy Studies** **Course Code: NCC2409L02-D**

| Teaching Scheme | | | | Evaluation Scheme | | | | |
|---|---|---|---|---|---|---|---|---|
| L | T | P | Cr | Exam | Theory % Marks | | Practical % Marks | |
| | | | | | Max | Min for Pass | Max | Min for Pass |
| 2 | 0 | 0 | 0 | CCA | 100 | 40 | - | - |
| 26 | 0 | | Total: 26 | | | | | |

**Category: Engineering Course**

**Prerequisites**:
Basic knowledge of how people learn and the psychological principles of education, Familiarity with Educational Practices

**Course Objectives:** Purposes of Course are:

5. To apply the foundational principles of pedagogy and their application in higher education.
6. To develop effective teaching strategies and methodologies.
7. To enhance skills in curriculum development and assessment.
8. To foster a reflective practice for continuous improvement in teaching.

**Course Outcomes:** After Successful completion of course units, students will

| | |
|---|---|
| CO1 | Appraise the theoretical foundations of pedagogy for higher education to create interest in learning |
| CO2 | Apply various teaching strategies and methods in learning environments to enhance competencies and skills in students |
| CO3 | Develop curriculum and assessment plans that align with learning objectives for fulfilling gaps in curriculum to make it more effective and ready for future requirements |
| CO4 | Reflect critically on their teaching practices and implement improvements in order to uplift learning outcomes achieved by students after every contact hour |

**Syllabus**

| Unit 1 | Foundations of Pedagogy | 07 hrs |
|---|---|---|
| Pedagogy Applied, Historical Perspectives on Education, Theories of Learning and Instruction, Cognitive, Social, and Constructivist Theories, Pedagogical Approaches: Teacher-Centered vs. Learner-Centered, Ethics and Values in Education | | |
| **Unit 2** | **Teaching Strategies and Methods** | **06 hrs** |

**FY M Tech VLSI and Embedded Systems, Semester I**

Instructional Design and Planning, Active Learning Strategies, Collaborative and Cooperative Learning, Technology-Enhanced Learning, Inclusive Teaching Practices, Classroom Management Techniques

| Unit 3 | Curriculum Development and Assessment | 07 hrs |
|---|---|---|

Curriculum Design Principles, Aligning Curriculum with Learning Outcomes, Formative and Summative Assessment Techniques, Designing Assessments for Diverse Learners, Feedback and its Role in Learning, Evaluating Teaching Effectiveness

| Unit 4 | Reflective Practice and Professional Development | 06 hrs |
|---|---|---|

Reflective Teaching Practices, Continuous Professional Development (CPD), Action Research in Education, Mentoring and Peer Observation, developing a Teaching Portfolio, Staying Updated with Educational Research

**Tutorials**

1) Create a group discussion on comparing various pedagogical theories and its suitability of applications

2) Prepare 4 mins effective video students to identify whether the scenario aligns with teacher-centered or learner-centered pedagogy.

3) Think-Pair and Share to design a lesson plan incorporating at least two active learning strategies differently for slow learners and advanced learners.

4) Present the curriculum plan and receive feedback from peers, the instructor and prepare modified plan.

**References Books:**


1. Illeris, K. (2018). *Contemporary Theories of Learning: Learning Theorists...in Their Own Words*. Routledge.
2. Brame, C. J. (2020). *Active Learning: Strategies to Promote Active Participation and Engagement*. Harvard University Press
3. Wiggins, G., & McTighe, J. (2020). *Understanding by Design*. ASCD
4. Brookfield, S. D. (2017). *Becoming a Critically Reflective Teacher*. Jossey-Bass


**Research Papers**


1. Sarkar, M., Gutierrez-Bucheli, L., Yip, S. Y., Lazarus, M., Wright, C., White, P. J., Ilic, D., Hiscox, T. J., & Berry, A. (2024). Pedagogical content knowledge (PCK) in higher education: A systematic scoping review. In Teaching and Teacher Education (Vol. 144, p. 104608). Elsevier BV. https://doi.org/10.1016/j.tate.2024.104608
2. Oje, A. V., Hunsu, N. J., & May, D. (2023). Virtual reality assisted engineering education: A multimedia learning perspective. In Computers & Education: X Reality (Vol. 3, p. 100033). Elsevier BV. https://doi.org/10.1016/j.cexr.2023.100033


**NPTEL/Swayam**

5. Outcome Based Pedagogic Principles for Effective Teaching - Prof. Dr. Shyamal Kumar Das Mandal - IIT Kharagpur

# D Y Patil College of Engineering, Akurdi, Pune

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester I

### Rubrics for Continuous Evaluation

| Component | Level | Unit 1 | Unit 2 | Unit 3 | Unit 4 | Total | Passing | Process Evaluation |
|---|---|---|---|---|---|---|---|---|
| Continuous Comprehensive Assessment (CCA) | Faculty | 25 | 25 | 25 | 25 | 100 | 40 | Refer CCA Guideline |

### CO-PO Mapping

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 3 | 3 | 3 | 2 | 2 | 3 |
| **CO2** | 3 | 3 | 2 | 3 | 3 | 3 |
| **CO3** | 3 | 2 | 1 | 1 | 3 | 3 |
| **CO4** | 3 | 2 | 1 | 3 | 3 | 3 |

3: High, 2: Moderate, 1: Low, 0/-: No Mapping

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# D Y Patil College of Engineering, Akurdi, Pune

An Autonomous Institute from AY 2024-25, Affiliated to Savitribai Phule Pune University, Pune

**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester II
## Syllabus Structure

| Course Code | Course | Teaching Scheme | | | | Evaluation Scheme | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | L | T | P | Cr | Exam | Theory % Marks | | | Practical % Marks | |
| | | | | | | | Max | Min for Pass | | Max | Min for Pass |
| VES2410L01 | Analog CMOS Design | 3 | 1 | 0 | 4 | CCA | 50 | 20 | 40 | - | - |
| | | | | | | ESE | 50 | 20 | | | |
| VES2410L02 | System on Chip | 3 | 1 | 0 | 4 | CCA | 50 | 20 | 40 | - | -- |
| | | | | | | ESE | 50 | 20 | | | |
| VES2410L03 | Embedded Automotive Systems | 3 | 1 | 0 | 4 | CCA | 50 | 20 | 40 | - | - |
| | | | | | | ESE | 50 | 20 | | | |
| VES2410L04 | Program Elective Course 2 | 3 | 1 | 0 | 4 | CCA | 50 | 20 | 40 | - | - |
| | | | | | | ESE | 50 | 20 | | | |
| VES2410P01 | Laboratory Practice II | 0 | 0 | 4 | 2 | CCA | - | - | | 50 | 20 |
| | | | | | | ESE | - | - | | 50 | 20 |
| VES2410P02 | Skill Development Course | 0 | 0 | 4 | 2 | CCA | - | - | | 100 | 40 |
| VES2410P03 | Industry based Mini Project | 0 | 0 | 4 | 2 | CCA | - | - | | 50 | 20 |
| | | | | | | ESE | - | - | | 50 | 20 |
| NCC2410L01 | Non Credit Course 2 | 2 | 0 | 0 | 0 | CCA | 100 | 40 | | Pass/Fail | |
| | **Total** | **14** | **4** | **12** | **22** | | | | | | |

| Program Elective Course 2 | |
|---|---|
| VES2410L04 | Embedded Product Design |
| VES2410L05 | High Speed ICs |
| VES2410L06 | Mixed Signal IC Design |
| VES2410L07 | Embedded Signal Processor Architectures |
| VES2410L08 | Real Time Operating Systems |

| Non Credit Course 2 | |
|---|---|
| NCC2410L01 | Stress Management by Yoga |
| NCC2410L02 | Personality Development through Life Enlightenment Skills |
| NCC2410L03 | IPR |

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**Department of Electronics and Telecommunication**

**FY M Tech VLSI and Embedded Systems, Semester II**

**Category: Program Core Course 4**

**Course Code: VES2410L01** **Course Title: Analog CMOS Design**

| Teaching Scheme | | | | Evaluation Scheme | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| L | T | P | Cr | Exam | Theory % Marks | | | Practical % Marks | |
| | | | | | Max | Min for Pass | | Max | Min for Pass |
| 3 | 1 | 0 | 4 | CCA | 50 | 40 | 40 | | |
| 39 | 13 | 0 | Total:52 | ESE | 50 | 40 | | | |

**Prerequisites:** Semiconductor physics, Analog circuit analysis, Linear Integrated Circuits, Digital CMOS Design

**Course Objectives:**

1. To understand theory of analog circuits using MOS small signal models
2. To understand design principles and techniques of CMOS Amplifiers
3. To gain design aspects of HF and Low Noise Amplifiers
4. To learn different methods of Stability and Frequency Compensation

**Course Outcomes :** After successful completion of the course the student will be able to:

| | |
|---|---|
| CO1 | Compare and contrast Simple MOS Large-Signal Model and Small-Signal Model for the MOS Transistor and modeling techniques. |
| CO2 | Design the current mirror circuits for various applications like differential amplifier and operational amplifier. |
| CO3 | Design and analyze various CMOS analog amplifiers, High Frequency and Low Frequency Noise Amplifiers. |
| CO4 | Design and analyze various stages of Operational amplifiers using CMOS devices. |
| CO5 | Design and construct two stage comparator and compare between the open loop and discrete time comparators using op-amp. |

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**Department of Electronics and Telecommunication**

**FY M Tech VLSI and Embedded Systems, Semester II**
**Syllabus**

| | | |
|---|---|---|
| **Unit I** | **MOS Devices and Modeling** | **7hrs** |
| MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Subthreshold MOS Model. | | |
| **Unit II** | **Analog CMOS Sub circuits** | **8hrs** |
| MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference. | | |
| **Unit III** | **CMOS Amplifiers, HF Amplifiers & Low Noise Amplifier** | **8hrs** |
| Design of CMOS amplifiers, Inverting amplifiers, Cascode amplifiers, Differential amplifiers, Folded cascade; Current amplifiers, Output amplifier.Open and Short circuit methods to estimate bandwidth, multistage amplifiers for high bandwidth, Low Noise Amplifier (LNA) design, Design of mixer, Advanced trends in Radio Frequency (RF) chip design. | | |
| **Unit IV** | **CMOS Operational Amplifiers** | **8hrs** |
| Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power-Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OPAmp. | | |
| **Unit V** | **Comparators** | **8hrs** |
| Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators. | | |
| **Reference Books** | | |
| 1. Thomas Lee, “The Design of CMOS Radio – Frequency Integrated Circuits”, Second edition, Cambridge.<br>2. Razavi B, “Design of Analog CMOS Integrated Circuits”, McGraw-Hill.<br>3. Allen P E and Holberg D R, CMOS Analog Circuit Design, Second Edition, Oxford University Press. | | |

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**Department of Electronics and Telecommunication**

**FY M Tech VLSI and Embedded Systems, Semester II**

**Tutorial**

| | | |
|---|---|---|
| **Unit I** | **Title: MOS Devices and Modeling** | **2 hrs** |
| Derive and compare the large-signal and Small-Signal Model for the MOS Transistor. | | |
| **Unit II** | **Title: Analog CMOS Sub circuits** | **3 hrs** |
| Simulate Current mirror circuits and analyze them using a SPICE simulator. The results should be compared with approximate manual calculations. As a result, write a report in which the simulations and calculations are discussed. | | |
| **Unit III** | **Title: CMOS Amplifiers, HF Amplifiers & Low Noise Amplifier** | **3 hrs** |
| Simulate the basic circuit of Inverting amplifiers, Cascode amplifiers, Differential amplifiers using SPICE simulator.<br><br>Implement Open and Short circuit methods to estimate bandwidth of Low Noise Amplifier. | | |
| **Unit IV** | **Title: CMOS Operational Amplifiers** | **3 hrs** |
| Design a Two-Stage Op Amps and derive its performance parameters. | | |
| **Unit V** | **Title: Comparators** | **2 hrs** |
| Compare the various types of comparators on the basis of different circuit performance metrics. | | |

# D Y Patil College of Engineering, Akurdi, Pune

An Autonomous Institute from AY 2024-25, Affiliated to Savitribai Phule Pune University, Pune

**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester II

### Rubrics for Continuous Evaluation

| Component | Level | Unit 1 | Unit 2 | Unit 3 | Unit 4 | Unit 5 | Total | Process Evaluation |
|---|---|---|---|---|---|---|---|---|
| Continuous Comprehensive Assessment (CCA) | Faculty | 10 | 10 | 10 | 10 | 10 | 50 | Refer CCA Guideline |
| End Semester Examination (ESE) | Institute | 10 | 10 | 10 | 10 | 10 | 50 | Each Unit Carries 10 marks Question |

### CO-PO Mapping

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 3 | 2 | 3 | 2 | 1 | 1 |
| **CO2** | 3 | 2 | 2 | 2 | 1 | 1 |
| **CO3** | 3 | 2 | 2 | 3 | 2 | 1 |
| **CO4** | 3 | 2 | 2 | 2 | 2 | 1 |
| **CO5** | 3 | 2 | 1 | 1 | 1 | - |

3: High, 2: Moderate, 1: Low, 0/-: No Mapping

# D Y Patil College of Engineering, Akurdi, Pune

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester II

**Category: Program Core Course 5**

**Course Code: VES2410L02** **Course Title: System On Chip**

| Teaching Scheme | | | | Evaluation Scheme | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| L | T | P | Cr | Exam | Theory % Marks | | | Practical % Marks | |
| | | | | | Max | Min for Pass | | Max | Min for Pass |
| 3 | 1 | 0 | 4 | CCA | 50 | 40 | 40 | | |
| 39 | 13 | 0 | Total:52 | ESE | 50 | 40 | | | |

**Prerequisites:** Digital CMOS Design, Microprocessor and Microcontroller, Embedded System Design

**Course Objectives:**

1. To understand the basic concepts and models in SoC
2. To explore Micro-programmed Architectures and SoC modeling
3. To explore features of simulation and synthesis of RTL intent
4. To learn recent trends in SoC design

**Course Outcomes:** After successful completion of the course the student will be able to:

| | |
|---|---|
| CO1 | Apply Design flow graphs flow modeling, finite state machine and simulation with RTL synthesis. |
| CO2 | Compose System on Chip modeling and hardware/software interfaces with respect to communication protocol |
| CO3 | Analyze memory architectures for System on Chip like internal and external memory . |
| CO4 | Appraise the SoC memory system design, embedded software and energy management techniques for SoC design, SoC prototyping, verification, testing and physical design. |
| CO5 | Design System on Chip using AES algorithms in image compression. |

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester II
## Syllabus

| | | |
|---|---|---|
| **Unit I** | **Basic Concepts** | **7hrs** |
| The nature of hardware and software, data flow modeling and implementation, the need for concurrent models, analyzing synchronous data flow graphs, control flow modeling and the limitations of data flow models, software and hardware implementation of data flow, analysis of control flow and data flow, Finite State Machine with data-path, cycle based bit parallel hardware, hardware model, FSMD data-path, simulation and RTL synthesis, language mapping for FSMD. | | |
| **Unit II** | **Micro-programmed Architectures** | **8hrs** |
| Limitations of FSM , Micro-programmed : control, encoding , data-path, Micro-programmed machine implementation , handling Micro-program interrupt and pipelining , General purpose embedded cores , processors, The RISC pipeline, program organization, analyzing the quality of compiled code, System on Chip, concept, design principles , portable multimedia system, SOC modeling, hardware/software interfaces , synchronization schemes, memory mapped Interfaces , co-processor interfaces, coprocessor control shell design, data and control design, Programmer's model . | | |
| **Unit III** | **Memory Design for SOC** | **8hrs** |
| Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I , and D – Caches , Multi Level Caches, Virtual to real translation , SOC Memory System , Models of Simple Processor – memory interaction. | | |
| **Unit IV** | **RTL intent** | **8hrs** |
| Simulation race, simulation-synthesis mismatch, timing analysis, timing parameters for digital logic, factors affecting delay and slew, sequential arcs, clock domain crossing, bus synchronization , preventing data loss through FIFO, Importance of low power, causes and factors affecting power, switching activity, simulation limitation, implication on synthesis and on backend. | | |
| **Unit V** | **Application Studies / Case Studies** | **8hrs** |
| SOC Design approach, AES algorithms, Design and evaluation, Image compression – JEPG compression. | | |

**Reference Books**


1. Patrick R. Schaumont, "A Practical Introduction to Hardware/Software Co-design", Springer Publications.
2. Sanjay Churiwala, Sapan Garg , "Principles of VLSI RTL Design A Practical Guide", Springer Publications.
3. Youn-Long Steve Lin, "Essential Issues in SOC Design, Designing Complex Systems-on Chip", Springer Publications.
4. Wayne Wolf, "Modern VLSI Design Systems on Chip", Pearson Education.
5. Rajanish K. Kamat, Santhosh A. Shinde, Vinod G. Shelake, "Unleash the System On Chip using FPGAs and Handel C", Springer Publications.

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**Department of Electronics and Telecommunication**

**FY M Tech VLSI and Embedded Systems, Semester II**

**Tutorial**

| | | |
|---|---|---|
| **Unit I** | **Title: Basic Concepts** | **2 hrs** |
| Determine a possible implementation for each of the following C statements in hardware. You can assume that all variables are integers and that each of them is stored in a register.<br>(a) a= a + 1;<br>(b) if (a > 20) a = 20;<br>(c) while (a < 20) a = a + 1 | | |
| **Unit II** | **Title: Micro-programmed Architectures** | **3 hrs** |
| Analyze the following terms:<br>a) Control hazard and data hazard<br>b) One-Way and Two-Way Handshake | | |
| **Unit III** | **Title: Memory Design for SOC** | **3 hrs** |
| Analyze various memories of SOC and explain in detail cache memory organization. | | |
| **Unit IV** | **Title: RTL intent** | **2 hrs** |
| Classify Bus Synchronization along with the Challenges in it and Enable Synchronization Method. | | |
| **Unit V** | **Title: Application Studies / Case Studies** | **3 hrs** |
| Judge the Design Issues and Techniques for image codec | | |

# D Y Patil College of Engineering, Akurdi, Pune

An Autonomous Institute from AY 2024-25, Affiliated to Savitribai Phule Pune University, Pune

**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester II
## Rubrics for Continuous Evaluation

| Component | Level | Unit 1 | Unit 2 | Unit 3 | Unit 4 | Unit 5 | Total | Process Evaluation |
|---|---|---|---|---|---|---|---|---|
| Continuous Comprehensive Assessment (CCA) | Faculty | 10 | 10 | 10 | 10 | 10 | 50 | Refer CCA Guideline |
| End Semester Examination (ESE) | Institute | 10 | 10 | 10 | 10 | 10 | 50 | Each Unit Carries 10 marks Question |

## CO-PO Mapping

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 3 | 2 | 3 | 2 | 1 | 2 |
| **CO2** | 3 | - | - | 2 | 1 | 1 |
| **CO3** | 3 | 2 | 2 | 2 | - | - |
| **CO4** | 3 | 2 | 2 | 3 | 2 | 1 |
| **CO5** | 3 | 2 | 1 | 2 | 1 | |

3: High, 2: Moderate, 1: Low, 0/-: No Mapping

# D Y Patil College of Engineering, Akurdi, Pune

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**Department of Electronics and Telecommunication**

**FY M Tech VLSI and Embedded Systems, Semester II**

**Category: Program Core Course 6**

**Course Code: VES2410L03** **Course Title: Embedded Automotive Systems**

| Teaching Scheme | | | | Evaluation Scheme | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| L | T | P | Cr | Exam | Theory % Marks | | | Practical % Marks | |
| | | | | | Max | Min for Pass | | Max | Min for Pass |
| 3 | 1 | 0 | 4 | CCA | 50 | 20 | 40 | - | - |
| Total Hours | | | | | | | | | |
| 39 | 13 | 0 | Total: 52 | ESE | 50 | 20 | | | |

**Prerequisites:** Embedded system Design

**Course Objectives:** After successful completion of the course the student will be able to:

1. To introduce the potential of automotive systems in industries
2. To understand Automotive Sensory Systems
3. To explain the importance of Automotive control in system design
4. To make students aware of different Automotive protocols for internal communication.

**Course Outcomes:** After successful completion of the course the student will be able to:

| | |
|---|---|
| CO1 | Analyze the fundamentals of different Automotive Systems in Automotive vehicle technology. |
| CO2 | Comprehend utility of sensors and instrumentation in vehicle systems like automotive sensors and transducers. |
| CO3 | Design control system for various vehicular modules like digital engine control, fuel control, EGR control. |
| CO4 | Interpret various control Modes of automotive Systems like cruise control system, electronic suspension system and electronic steering control. |
| CO5 | Illustrate the various automotive protocols such as LIN, CAN, KWP2000 and J1939, FlexRay and use of vehicle calibration tools |

# D Y Patil College of Engineering, Akurdi, Pune

An Autonomous Institute from AY 2024-25, Affiliated to Savitribai Phule Pune University, Pune

**Department of Electronics and Telecommunication**

**FY M Tech VLSI and Embedded Systems, Semester II**
**Syllabus**

| | | |
|---|---|---|
| **Unit I** | **Automotive Systems Overview** | **7 hrs** |
| Automotive Vehicle Technology, Overview of Vehicle Categories, Various Vehicle Sub Systems like Chassis, Body, Driveline, Engine technology, Fuelling technology, vehicle Emission, Brakes, Suspension, Emission, Doors, Dashboard instruments, Wiring Harness, Safety & Security, Comfort & Infotainment, Communication & Lighting, Future Trends in Automotive Embedded Systems: Hybrid Vehicles, Electric Vehicles. | | |
| **Unit II** | **Automotive Sensory System** | **8 hrs** |
| Automotive Sensors and Transducers: Temperature, Manifold and Barometric Pressures, Humidity, Carbon Dioxide (CO2), Carbon Monoxide (CO), Oxygen (O2) Sensor, Proximity Distance Sensors, Engine Speed sensor, Throttle Position Sensor, Pressure Sensors, Knock Sensor & Mass Flow Sensor. Typical Sensors Specifications & Microcontroller Interface Considerations, Sensor Calibration, Curve fitting. | | |
| **Unit III** | **Automotive Control System Design** | **8 hrs** |
| Digital Engine Control, Features, Control Modes for Fuel Control, Discrete Time Idle Speed Control, EGR Control, Variable Valve Timing Control, Electronic Ignition Control, Integrated Engine Control System. | | |
| **Unit IV** | **Control Modes** | **8 hrs** |
| Summary of Control Modes, Cruise Control System, Cruise Control Electronics, Anti-locking Braking System, Electronic Suspension System, Electronic Steering Control, Four-Wheel Steering. | | |
| **Unit V** | **Automotive Protocols and Calibration and Diagnostics Tools** | **8 hrs** |
| The need for Protocol, Automotive Protocols: LIN, CAN, KWP2000 and J1939, FlexRay, Test, Calibration and Diagnostics tools for networking of electronic systems like ECU Software and Testing Tools, ECU Calibration Tools | | |
| **Reference Books** | | |
| 1. William B. Ribbens, "Understanding Automotive Electronics- An Engineering Perspective", Seventh edition, Butterworth-Heinemann Publications.<br>2. Ronald K. Jurgen, "Automotive Electronics Handbook", Mc-Graw Hill.<br>3. Kiencke, Uwe, Nielsen & Lars, "Automotive Control Systems for Engine, Driveline and Vehicle", Second edition, Springer Publication.<br>4. Tao Zhang, Luca Delgrossi, "Vehicle Safety Communications: Protocols, Security and Privacy", Wiley Publication. | | |

# D Y Patil College of Engineering, Akurdi, Pune

An Autonomous Institute from AY 2024-25, Affiliated to Savitribai Phule Pune University, Pune

**Department of Electronics and Telecommunication**

**FY M Tech VLSI and Embedded Systems, Semester II**

**Tutorial**

| | | |
|---|---|---|
| **Unit I** | **Title: Automotive Systems Overview** | **2 hrs** |
| Determine the various operating models and compare advantages and disadvantages of each.<br>Assess the working of spark plug & disk braking systems with suitable diagrams. | | |
| **Unit II** | **Title: Automotive Sensory System** | **2 hrs** |
| Examine with a suitable diagram Fuel Injectors in Petrol engine along with the security& warning system.<br><br>Inspect the selection criteria of sensors for automotive applications like RADARranging and telematics. | | |
| **Unit III** | **Title: Automotive Control System Design** | **3 hrs** |
| Compare the electronics steering control system and automatic rain operated wiper control.<br><br>Propose the superset of variables sensed in engine control system | | |
| **Unit IV** | **Title: Control Modes** | **3 hrs** |
| Examine the role of control system strategies in fine tuning an automotive system?<br><br>Present the components of an electronically controlled engine with suitable diagrams.<br><br>Compare analog & digital cruise control systems. | | |
| **Unit V** | **Title: Automotive Protocols and Calibration and Diagnostics Tools** | **3 hrs** |
| Demonstrate protocol wakeup & startup with respect to FlexRay protocol.<br><br>Construct connection schematic of CAN centrate & ReCANcentrate.<br><br>Compare LIN & Flex Ray with respect to automotive applications.<br><br>Relate the importance of calibrated test equipment? Hence make use of vehiclecalibration tools. | | |

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An Autonomous Institute from AY 2024-25, Affiliated to Savitribai Phule Pune University, Pune

**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester II

### Rubrics for Continuous Evaluation

| Component | Level | Unit 1 | Unit 2 | Unit 3 | Unit 4 | Unit 5 | Total | Process Evaluation |
|---|---|---|---|---|---|---|---|---|
| Continuous Comprehensive Assessment (CCA) | Faculty | 10 | 10 | 10 | 10 | 10 | 50 | Refer CCA Guideline |
| End Semester Examination (ESE) | Institute | 10 | 10 | 10 | 10 | 10 | 50 | Each Unit Carries 10 marks Question |

### CO-PO Mapping

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 3 | 2 | 3 | 2 | 2 | 2 |
| **CO2** | 3 | 3 | 2 | 2 | 1 | 2 |
| **CO3** | 3 | 2 | 2 | 1 | 1 | 2 |
| **CO4** | 3 | 2 | 2 | 2 | 2 | 1 |
| **CO5** | 3 | 2 | 2 | 1 | 1 | - |

3: High, 2: Moderate, 1: Low, 0/-: No Mapping

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# D Y Patil College of Engineering, Akurdi, Pune

An Autonomous Institute from AY 2024-25, Affiliated to Savitribai Phule Pune University, Pune

**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester II

**Category: Program Elective Course 2**

**Course Code: VES2410L04** **Course Title: Embedded Product Design**

| Teaching Scheme | | | | Evaluation Scheme | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| L | T | P | Cr | Exam | Theory % Marks | | | Practical % Marks | |
| | | | | | Max | Min for Pass | | Max | Min for Pass |
| 3 | 1 | 0 | 4 | CCA | 50 | 20 | 40 | - | - |
| Total Hours | | | | | | | | | |
| 39 | 13 | 0 | Total: 52 | ESE | 50 | 20 | | | |

**Prerequisites:** Embedded System Design, Processor Design

**Course Objectives:** After successful completion of the course the student will be able to:

1. To understand design challenges of embedded hardware and software
2. To gain knowledge of testing and verification issues in design cycle
3. To introduce h/w and s/w design models with different technology
4. To learn the importance of documentation for technology transfer

**Course Outcomes :**Student will:

| | |
|---|---|
| CO1 | Distinguish specifications and design challenges of embedded products. |
| CO2 | Estimate cost of embedded product for cost efficient product design. |
| CO3 | Demonstrate the knowledge of embedded product design related software design tools |
| CO4 | Develop design technology using hardware design, validation and maintenance. |
| CO5 | Analyze the aspects of Mechanical Packaging, Testing, reliability and failure analysis |

# D Y Patil College of Engineering, Akurdi, Pune

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester II
## Syllabus

| | | |
|---|---|---|
| **Unit I** | **Overview of Embedded Products** | **7hrs** |
| Need, Design challenges, product survey, specifications of product need of hardware and software, Partitioning of the design into its software and hardware components, Iteration and refinement of the partitioning. | | |
| **Unit II** | **Design Models and Techniques** | **8hrs** |
| Various models of development of hardware and software, their features, different Processor technology, IC technology, Design Technology. | | |
| **Unit III** | **Modules of Software** | **8hrs** |
| Tradeoffs, Custom Single-purpose processors, General Purpose processors, Software, Memory, Interfacing | | |
| **Unit IV** | **Design Technology** | **8hrs** |
| Hardware design, FPGA design, firmware design, driver development, RTOS porting, cost reduction, reengineering, optimization, maintenance, validation and development, prototyping, turnkey product design | | |
| **Unit V** | **Testing and Verification** | **8hrs** |
| Embedded products-areas of technology, Design and verification, Integration of the hardware and software components, testing- different tools, their selection criterion. | | |
| **Reference Books** | | |
| 1 Vahid Frank and Tony Givargis , “Embedded System Design: A Unified Hardware/Software Introduction”, John Wiley Publication.<br>2 Marwedel P, “Embedded System Design”, Springer Publication. | | |

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**Department of Electronics and Telecommunication**

**FY M Tech VLSI and Embedded Systems, Semester II**

**Tutorial**

| | | |
|---|---|---|
| **Unit I** | **Title: Overview of Embedded Products** | **2 hrs** |
| Appraise the needs of software and software partitioning in embedded product design. | | |
| **Unit II** | **Title: Design Models and Techniques** | **2 hrs** |
| Compare different processor Technology, IC Technology and Design Technology. | | |
| **Unit III** | **Title: Modules of Software** | **3 hrs** |
| Demonstrate software and memory Interfacing used for computer system design with a neat Sketch diagram. | | |
| **Unit IV** | **Title: Design Technology** | **3 hrs** |
| Identify and emphasize the different Embedded Product design Technologies useful for industrial automation, Internet of Things and innovative technology integration. | | |
| **Unit V** | **Title: Testing and Verification** | **3 hrs** |
| Compare different Testing & Verification tools used in Embedded Product Design such as static analysis and dynamic analysis. | | |

# D Y Patil College of Engineering, Akurdi, Pune

An Autonomous Institute from AY 2024-25, Affiliated to Savitribai Phule Pune University, Pune

**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester II

### Rubrics for Continuous Evaluation

| Component | Level | Unit 1 | Unit 2 | Unit 3 | Unit 4 | Unit 5 | Total | Process Evaluation |
|---|---|---|---|---|---|---|---|---|
| Continuous Comprehensive Assessment (CCA) | Faculty | 10 | 10 | 10 | 10 | 10 | 50 | Refer CCA Guideline |
| End Semester Examination (ESE) | Institute | 10 | 10 | 10 | 10 | 10 | 50 | Each Unit Carries 10 marks Question |

### CO-PO Mapping

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 3 | 2 | 3 | 2 | 1 | 1 |
| **CO2** | 3 | - | - | 2 | 1 | - |
| **CO3** | 3 | 2 | 2 | 1 | - | - |
| **CO4** | 3 | 2 | 2 | 2 | 2 | 1 |
| **CO5** | 3 | 2 | 1 | 1 | 1 | 1 |

3: High, 2: Moderate, 1: Low, 0/-: No Mapping

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# D Y Patil College of Engineering, Akurdi, Pune

An Autonomous Institute from AY 2024-25, Affiliated to Savitribai Phule Pune University, Pune

**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester II

**Category: Program Elective Course 2**

**Course Code: VES2410L05** **Course Title: High Speed ICs**

| Teaching Scheme | | | | Evaluation Scheme | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| L | T | P | Cr | Exam | Theory % Marks | | | Practical % Marks | |
| | | | | | Max | Min for Pass | | Max | Min for Pass |
| 3 | 1 | 0 | 4 | CCA | 50 | 20 | 40 | - | - |
| Total Hours | | | | | | | | | |
| 39 | 13 | 0 | Total: 52 | ESE | 50 | 20 | | | |

**Prerequisites:** Digital CMOS Design, Analog CMOS Design, System on Chip

**Course Objectives:**

1. To understand basic design aspects of high frequency circuits
2. To explain different characteristics of high speed logic families
3. To learn design issues of interconnects in High Speed Circuit Design

**Course Outcomes :** After successful completion of the course the student will be able to:

| | |
|---|---|
| CO1 | Analyze details about High Speed VLSI Circuits Design like high frequency circuits in wireless and fiber optic systems. |
| CO2 | Identify the basic need of high speed digital logic families such as Bi-CMOS MOS-HBT logic, Pseudo-CML logic, Other bipolar, MOS and Bi-CMOS CML, and ECL gates. |
| CO3 | Justify various types of VLSI interconnections like Single level interconnections and parallel multi level interconnections. |
| CO4 | Analyze various interconnection delay models for microstrip interconnections and Multilayer Integrated circuits. |
| CO5 | Evaluate high speed circuit designs with respect to crosstalk due to connectors, near and far end crosstalk and cross talk in terminators and also acquire insights of IC packaging. |

# D Y Patil College of Engineering, Akurdi, Pune

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester II
## Syllabus

| | | |
|---|---|---|
| **Unit I** | **Overview of high-frequency ICs** | **7 hrs** |
| A brief history of high-frequency integrated circuits and its design, High-frequency circuits in wireless, fiber-optic and imaging systems. | | |
| **Unit II** | **High speed digital logic families** | **8 hrs** |
| High-speed digital logic families, Design methodology for maximum data rate, Bi-CMOS MOS-HBT logic, Pseudo-CML logic, Other bipolar, MOS and Bi-CMOS CML, and ECL gates, CML/ECL gate layout techniques. | | |
| **Unit III** | **VLSI interconnections** | **8 hrs** |
| Metal-Insulator-Semiconductor Microstrip Line Model of an Interconnection., Transmission Line Analysis of Single Level Interconnections, Transmission Line Analysis of Parallel Multilevel Interconnections | | |
| **Unit IV** | **Interconnections delay model** | **8 hrs** |
| Very High Frequency Losses in a Microstrip Interconnection, Compact Expressions for Interconnection Delays, Interconnection Delays in Multilayer Integrated Circuits | | |
| **Unit V** | **High Speed Circuit Design and IC Packaging** | **8 hrs** |
| High Speed Properties of logic gates-power, speed and packaging. Cross talk in solid ground and slotted ground planes, Near end and Far end crosstalk. End terminators and cross talk in terminators.<br>IC packaging - Requirements and properties; materials and substrates; wire-bonding; chip and wafer-level packaging; impact on reliability and testability. | | |
| **Reference Books** | | |
| 1. VoinigescuSorin, “High-Frequency Integrated Circuits”, Cambridge University Press.<br>2. Goel A K , “High-Speed VLSI Interconnections”, Second edition, Wiley-IEEE Press.<br>3. Nakhla M S, Zhang O J, “Modeling and Simulation of High Speed VLSI Interconnects”, Springer Publication.<br>4. Ludwig Reinhold, Bretchko Pavel, “RF Circuit Design Theory and Applications”, Pearson education.<br>5. Howard Johnson, Graham Martin, “High Speed digital Design-A Handbook of Black Magic”, Pearson education. | | |

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**Department of Electronics and Telecommunication**

**FY M Tech VLSI and Embedded Systems, Semester II**

**Tutorial**

| | | |
|---|---|---|
| **Unit I** | **Title: Frequency analysis for high freq ICs** | **2 hrs** |
| Analyze different wireless high frequency operating circuits that enable high speed data transmission using power lines. | | |
| **Unit II** | **Title: High speed Digital CMOS logic families** | **3 hrs** |
| Evaluate CMOS based ECL and bipolar devices with respect to sensitivity and specific detection of analytics with low background noise. | | |
| **Unit III** | **Title: Interconnection in VLSI model** | **2 hrs** |
| Justify the different types of errors in interconnection relevant to power consumption, timing closure, physical design etc. | | |
| **Unit IV** | **Title: Delays due to interconnection** | **3 hrs** |
| Design and analyze delays occurring due to interconnection like network delay, transition delay and path delay. | | |
| **Unit V** | **Title: High Speed Circuit Design and IC Packaging** | **3 hrs** |
| Analyze and elaborate different types of crosstalk such as positive and negative crosstalk.<br>Compare between chip and wafer-level packaging. | | |

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester II

### Rubrics for Continuous Evaluation

| Component | Level | Unit 1 | Unit 2 | Unit 3 | Unit 4 | Unit 5 | Total | Process Evaluation |
|---|---|---|---|---|---|---|---|---|
| Continuous Comprehensive Assessment (CCA) | Faculty | 10 | 10 | 10 | 10 | 10 | 50 | Refer CCA Guideline |
| End Semester Examination (ESE) | Institute | 10 | 10 | 10 | 10 | 10 | 50 | Each Unit Carries 10 marks Question |

### CO-PO Mapping

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 3 | 2 | 3 | - | 3 | - |
| **CO2** | 3 | - | - | - | - | 2 |
| **CO3** | 3 | 2 | 2 | 1 | - | - |
| **CO4** | 3 | 2 | 2 | - | 2 | 1 |
| **CO5** | 3 | 2 | 2 | 3 | 2 | 2 |

3: High, 2: Moderate, 1: Low, 0/-: No Mapping

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# D Y Patil College of Engineering, Akurdi, Pune

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**Department of Electronics and Telecommunication**

**FY M Tech VLSI and Embedded Systems, Semester II**

**Category: Program Elective Course 2**

**Course Code: VES2410L06** **Course Title: Mixed Signal IC Design**

| Teaching Scheme | | | | Evaluation Scheme | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| L | T | P | Cr | Exam | Theory % Marks | | | Practical % Marks | |
| | | | | | Max | Min for Pass | | Max | Min for Pass |
| 3 | 1 | 0 | 4 | CCA | 50 | 20 | 40 | - | - |
| Total Hours | | | | | | | | | |
| 39 | 13 | 0 | Total: 52 | ESE | 50 | 20 | | | |

**Prerequisites:** Digital CMOS Design, Analog CMOS Design, System on Chip

**Course Objectives:**

1. To introduced Mixed Signal layout issues in circuit design
2. To explain the Architectures of ADC and DAC
3. To acquire knowledge on Modeling Data Convertors

**Course Outcomes :** After successful completion of the course the student will be able to:

| | |
|---|---|
| CO1 | Elaborate the mixed signal issues in circuit design like floor planning, power supply and grounding issues and interconnect considerations. |
| CO2 | Design models for different ADC systems such as successive approximation, dual slope and pipeline. |
| CO3 | Inspect data converter modeling methodologies like time domain description of reconstruction. |
| CO4 | Apply methods to improve SNR like spectral density view, jitter and averaging. |
| CO5 | Evaluate the operation of delta-sigma/ sigma-delta converters and their issues. |

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**Department of Electronics and Telecommunication**

**FY M Tech VLSI and Embedded Systems, Semester II**
**Syllabus**

| | | |
|---|---|---|
| **Unit I** | **Analog and Discrete Time Signals** | **7hrs** |
| Analog versus discrete time signals, converting analog signal to digital signal, Sample and hold characteristics, DAC specifications, ADC specifications, Mixed signal layout issues: floor planning, power supply and grounding issues, fully differential design/ matching, guard rings, shielding, interconnect considerations**.** | | |
| **Unit II** | **ADC Architectures** | **8hrs** |
| Resistor string, R-2R ladder networks, Current steering, Charge-scaling, Pipeline. ADC architectures: Flash, Pipeline, Dual slope, Successive approximation, Oversampling ADC. | | |
| **Unit III** | **Data converter modeling** | **8hrs** |
| Sampling and aliasing: A modeling approach, Impulse sampling, AAF and RCF, Time domain description of reconstruction, The sample and hold, S/H spectral response, Circuit concerns for implementing S/H | | |
| **Unit IV** | **Noise improvement** | **8hrs** |
| Quantization noise, RMS quantization noise voltage, treating quantization noise as a random variable, calculating RMS quantization noise voltage from a spectrum | | |
| **Unit V** | **Data converter SNR** | **8hrs** |
| Effective number of bits, Signal to noise plus distortion ratio, Spurious free dynamic range, dynamic range, SNR & SNDR, Clock jitter, Averaging to improve SNR, Spectral density view, Jitter and averaging | | |
| **Reference Books** | | |
| 1. Baker R J, "CMOS: Mixed Signal Circuit Design", Second edition, Wiley IEEE Press Publications.<br>2. Baker R J, "CMOS: Circuit Design, Layout and Simulation", Second edition, Wiley IEEE Press Publications.<br>3. Allen, Phillip E., Holberg, Douglus R., "CMOS Analog Circuit Design", Oxford University Press Publications. | | |

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester II

**Tutorial**

| | | |
|---|---|---|
| **Unit I** | **Title: Analog and Discrete Time Signals** | **2 hrs** |
| Elaborate ground bounce and power supply issue in Analog to Digital converter. | | |
| **Unit II** | **Title: ADC Architectures** | **2 hrs** |
| Evaluate successive approximation ADC blocks like flash, pipeline, dual slope and oversampling ADC. | | |
| **Unit III** | **Title: Data converter modeling** | **3 hrs** |
| Design and sample and hold circuit for electronics system using time domain description and reconstruction. | | |
| **Unit IV** | **Title: Noise improvement** | **3 hrs** |
| Evaluate how to Quantize noise measurement from spectrum by treating quantization of noise as a random variable and calculating RMS quantization noise voltage from spectrum. | | |
| **Unit V** | **Title: Data converter SNR** | **3 hrs** |
| Analyze Spurious free dynamic range in Digital to Analog converter. | | |

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester II

### Rubrics for Continuous Evaluation

| Component | Level | Unit 1 | Unit 2 | Unit 3 | Unit 4 | Unit 5 | Total | Process Evaluation |
|---|---|---|---|---|---|---|---|---|
| Continuous Comprehensive Assessment (CCA) | Faculty | 10 | 10 | 10 | 10 | 10 | 50 | Refer CCA Guideline |
| End Semester Examination (ESE) | Institute | 10 | 10 | 10 | 10 | 10 | 50 | Each Unit Carries 10 marks Question |

### CO-PO Mapping

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 3 | 2 | 3 | 2 | 1 | 2 |
| **CO2** | 3 | - | - | 2 | 1 | 2 |
| **CO3** | 3 | 2 | 2 | 3 | 1 | - |
| **CO4** | 3 | 2 | 2 | 2 | 2 | 1 |
| **CO5** | 3 | 2 | 2 | 2 | 1 | 2 |

3: High, 2: Moderate, 1: Low, 0/-: No Mapping

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# D Y Patil College of Engineering, Akurdi, Pune

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester II

**Category: Program Elective Course 2**

**Course Code: VES2410L07 Course Title: Embedded Signal Processor Architectures**

| Teaching Scheme | | | | Evaluation Scheme | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| L | T | P | Cr | Exam | Theory % Marks | | | Practical % Marks | |
| | | | | | Max | Min for Pass | | Max | Min for Pass |
| 3 | 1 | 0 | 4 | CCA | 50 | 20 | 40 | - | - |
| Total Hours | | | | | | | | | |
| 39 | 13 | 0 | Total: 52 | ESE | 50 | 20 | | | |

**Prerequisites:** Embedded System Design, Processor Design, Digital Signal Processing

**Course Objectives:**

1. To impart knowledge on the theoretical aspects of signal analysis and processing
2. To explore DSP Processor architectures
3. To understand DSP algorithms
4. To elaborate real world DSP applications

**Course Outcomes :** After successful completion of the course the student will be able to:

| | |
|---|---|
| CO1 | Analyze DSP system with linear filters using DFT |
| CO2 | Develop technical abilities of designing any applications with FIR and IIR filters |
| CO3 | Apply different memory management technique &Port algorithms like paging , swapping, segmentation and compaction on DSP Processor Platforms |
| CO4 | Elaborate different representation techniques of DSP algorithms such as data flow graph and signal flow graph. |
| CO5 | Analyze filter structures with practical applications of DSP like audio and speech processing, sonar, radar and other sensor array processing. |

# D Y Patil College of Engineering, Akurdi, Pune

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**Department of Electronics and Telecommunication**

**FY M Tech VLSI and Embedded Systems, Semester II**
**Syllabus**

| | | |
|---|---|---|
| **Unit I** | **Signal Analysis and Processing** | **7 hrs** |
| Discrete Fourier Transform, Fast Fourier Transform, Design of FIR Filters using windowing technique, Design of IIR Filters through Impulse invariance and bilinear transformation technique, Algorithms of Adaptive Filters, Design and Applications of Adaptive Filters. | | |
| **Unit II** | **Introduction to Digital signal processing systems** | **8 hrs** |
| MAC, Barrel shifter, ALU, Multipliers, Dividers, DSP processor architecture, Software developments, Selections of DSP processors, Hardware interfacing | | |
| **Unit III** | **DSP processor architectures** | **8 hrs** |
| TMS320C54XX, TMS320C67XX, Blackfin processor: Architecture overview, memory management, I/O management, Real time implementation Considerations, Memory System and Data Transfer, Code Optimization. | | |
| **Unit IV** | **Representations of the DSP algorithms** | **8 hrs** |
| Block diagrams, Signal flow graph, Data-flow graph, Dependence graph. Iteration bounds: Critical Path, Loop Bound, Algorithm to compute iteration bound, Longest Path Matrix (LPM). | | |
| **Unit V** | **Practical DSP Applications** | **8 hrs** |
| Audio Coding and Audio Effects, Digital Image Processing, Two-Dimensional Filtering, Image Enhancement, DTMF generation and detection, FFT algorithms, Wavelet algorithms | | |
| **Reference Books** | | |


1. Woon-SengGan, Sen M. Kuo, “Embedded Signal Processing With the Micro Signal Architecture”, Wiley-IEEE Press.
2. KuoSen M, Woon-SengGan,“ Digital Signal Processors: Architectures, Implementations and Applications”, Prentice-Hall.
3. Proakis J G, Manolakis D G, “Digital Signal Processing, Principles, Algorithms and Applications”, Prentice-Hall.
4. Lawrence R. R, Bernard Gold, “Theory and Application of Digital signal Processing”, Prentice-Hall.
5. ParhiKeshab , “VLSI Digital Signal Processing System”, Wiley Publication.

# D Y Patil College of Engineering, Akurdi, Pune

An Autonomous Institute from AY 2024-25, Affiliated to Savitribai Phule Pune University, Pune

**Department of Electronics and Telecommunication**

**FY M Tech VLSI and Embedded Systems, Semester II**

**Tutorial**

| | | |
|---|---|---|
| **Unit I** | **Title: Signal Analysis and Processing** | **2 hrs** |
| 1. Elaborate on Design of FIR Filters using windowing technique<br>2. Develop the Design of IIR Filters through Impulse invariance and bilinear transformation technique<br>3. Solve DFT of a sequence x(n) = { 0,1,2,4,,6,8,7,3} using DIFFFT algorithm | | |
| **Unit II** | **Title: Introduction to Digital signal processing systems** | **2 hrs** |
| 1. With neat sketch elaborate the computational building blocks of DSP | | |
| **Unit III** | **Title: DSP processor architectures** | **3 hrs** |
| 1. Draw and elaborate the block diagram of memory interface for TMS320C54XX processor<br>2. Compare the Blackfin processor with TMS320C6713. | | |
| **Unit IV** | **Title: Representations of the DSP algorithms** | **3 hrs** |
| 1. Compare and contrast between signal flow graph & Data flow graph<br>2. Determine algorithm to compute iteration bound | | |
| **Unit V** | **Title: Practical DSP Applications** | **3 hrs** |
| 1. Elaborate on how DSP processors can be used in Image enhancement<br>2. Classify DTMF generation and detection | | |

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester II
## Rubrics for Continuous Evaluation

| Component | Level | Unit 1 | Unit 2 | Unit 3 | Unit 4 | Unit 5 | Total | Process Evaluation |
|---|---|---|---|---|---|---|---|---|
| Continuous Comprehensive Assessment (CCA) | Faculty | 10 | 10 | 10 | 10 | 10 | 50 | Refer CCA Guideline |
| End Semester Examination (ESE) | Institute | 10 | 10 | 10 | 10 | 10 | 50 | Each Unit Carries 10 marks Question |

## CO-PO Mapping

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 3 | 2 | 3 | 3 | 1 | 1 |
| **CO2** | 3 | - | - | 2 | 2 | - |
| **CO3** | 3 | 2 | 2 | 1 | 2 | - |
| **CO4** | 3 | 2 | 2 | 2 | - | 1 |
| **CO5** | 3 | 2 | 1 | 1 | 1 | 2 |

3: High, 2: Moderate, 1: Low, 0/-: No Mapping

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# D Y Patil College of Engineering, Akurdi, Pune

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester II

**Category: Program Elective Course 2**

**Course Code: VES2410L08** **Course Title: Real Time Operating System**

| Teaching Scheme | | | | Evaluation Scheme | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| L | T | P | Cr | Exam | Theory % Marks | | | Practical % Marks | |
| | | | | | Max | Min for Pass | | Max | Min for Pass |
| 3 | 1 | 0 | 4 | CCA | 50 | 20 | 40 | - | - |
| Total Hours | | | | | | | | | |
| 39 | 13 | 0 | Total: 52 | ESE | 50 | 20 | | | |

**Prerequisites:** Embedded System Design, Operating System

**Course Objectives:**

1. To understand software Architecture and Development cycle of Operating Systems
2. To learn various management attributes of Operating System
3. To understand RTOS
4. To study Linux/ RT Linux environment

**Course Outcomes :** After successful completion of the course the student will be able to:

| | |
|---|---|
| CO1 | Analyze Embedded Software Developments Tools |
| CO2 | Demonstrate Life Cycle of Software Development Process |
| CO3 | Evaluate different Monolithic systems |
| CO4 | Design a simple RTOS kernel structure inspired by μC/OS |
| CO5 | Evaluate the impact of the Linux kernel's modularity on system performance and flexibility and Analyze the advantages of using semaphores over mutexes in certain synchronizationscenarios. |

# D Y Patil College of Engineering, Akurdi, Pune

An Autonomous Institute from AY 2024-25, Affiliated to Savitribai Phule Pune University, Pune

**Department of Electronics and Telecommunication**

**FY M Tech VLSI and Embedded Systems, Semester II**
**Syllabus**

| | | |
|---|---|---|
| **Unit I** | **List of software development tools** | **7 hrs** |
| Software Architectures, Software Developments Tools, Programming Concepts, Embedded Programming in C and C++, Queues, Stacks, Optimization of Memory needs, Program Modeling Concepts, Software Development Process Life Cycle and its Model, Software Analysis, Design and Maintenance | | |
| **Unit II** | **Life Cycle of Software Development Process** | **8 hrs** |
| Operating System Concepts, Processes, Deadlocks, Memory Management, Input /Output, Files, Security, the Shell, Recycling of Concepts. | | |
| **Unit III** | **Monolithic Systems** | **8 hrs** |
| Operating system structure Monolithic Systems: Layered Systems, Virtual Machines, Exo-kernels, Client-Server Model | | |
| **Unit IV** | **Multitasking in µCOS** | **8 hrs** |
| Real Time Operating Systems (µC/OS):Real-Time Software Concepts, Kernel Structure, Task Management, Time Management, Inter task Communication & Synchronization, Memory Management, and Porting µCos-II. | | |
| **Unit V** | **Linux Operating system and Semaphore for signaling and synchronization** | **8 hrs** |
| Linux/RT Linux: Features of Linux, Linux commands, File Manipulations, Directory, Pipes and Filters, File Protections, Shell Programming.<br>System Programming, RT Linux Modules, POSIX Threads, Mutex Management, Semaphore Management. | | |
| **Reference Books** | | |


1. Labrossy J. J, Lawrence, "µC/OS-II, The real time Kernel", R & D Publication.
2. Dr Prasad K V K K, "Embedded Real Time Systems: Concepts, Design & Programming", Dreamtech Publication.
3. Simon D. E, "An Embedded Software Primer", Pearson education.
4. Tanenbaum A S, "Modern Operating Systems", Prentice Hall.
5. Raj Kamal, "Embedded Systems Architecture, Programming and design", Tata Mc-Graw-Hill.

# D Y Patil College of Engineering, Akurdi, Pune

An Autonomous Institute from AY 2024-25, Affiliated to Savitribai Phule Pune University, Pune

**Department of Electronics and Telecommunication**

**FY M Tech VLSI and Embedded Systems, Semester II**

**Tutorial**

| | | |
|---|---|---|
| **Unit I** | **Title: List of software development tools** | **2 hrs** |
| 1. Compare and contrast the features of various development tools.<br>2. Design embedded software for specific applications.<br>3. Design a custom SDLC model for a specific project. | | |
| **Unit II** | **Title: Life Cycle of Software Development Process** | **2 hrs** |
| 1. Design a basic structure for a hypothetical operating system with essential features.<br>2. Distinguish between a process and a thread.<br>3. Identify different types of I/O devices and their roles in a computer system. | | |
| **Unit III** | **Title: Monolithic Systems** | **3 hrs** |
| 1. Analyze the advantages and disadvantages of using a monolithic kernel in an operating system.<br>2. Design a simple monolithic kernel for a hypothetical operating system.<br>3. Demonstrate how to organize the components of an operating system into layers. | | |
| **Unit IV** | **Title: Multitasking in µCOS** | **3 hrs** |
| 1. Compare the µC/OS-II kernel structure with that of another RTOS.<br>2. Design a task management system for a real-time application using µC/OS-II.<br>3. Describe the steps involved in porting µC/OS-II to a new hardware platform. | | |
| **Unit V** | **Title: Linux Operating system and Semaphore for signaling and synchronization** | **3 hrs** |
| 1. Analyze the differences between the cp, mv, and rsync commands in terms of file management.<br>2. Explain how the cat, less, and nano commands are used to view and edit files. | | |

3. Describe the structure of a typical Linux directory hierarchy.

4. Design a pipeline that processes a log file to extract and count error messages.

5. Design an RT Linux module that handles a specific real-time task, such as precise timing control for an industrial application.

# D Y Patil College of Engineering, Akurdi, Pune

An Autonomous Institute from AY 2024-25, Affiliated to Savitribai Phule Pune University, Pune

**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester II
## Rubrics for Continuous Evaluation

| Component | Level | Unit 1 | Unit 2 | Unit 3 | Unit 4 | Unit 5 | Total | Process Evaluation |
|---|---|---|---|---|---|---|---|---|
| Continuous Comprehensive Assessment (CCA) | Faculty | 10 | 10 | 10 | 10 | 10 | 50 | Refer CCA Guideline |
| End Semester Examination (ESE) | Institute | 10 | 10 | 10 | 10 | 10 | 50 | Each Unit Carries 10 marks Question |

## CO-PO Mapping

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 3 | 2 | 2 | 3 | 2 | - |
| **CO2** | 2 | 2 | 2 | 3 | 2 | 2 |
| **CO3** | 2 | 2 | 2 | 1 | 1 | - |
| **CO4** | 3 | 2 | 2 | 2 | 2 | 1 |
| **CO5** | 3 | 3 | 2 | 1 | 1 | - |

3: High, 2: Moderate, 1: Low, 0/-: No Mapping

*****

# D Y Patil College of Engineering, Akurdi, Pune

An Autonomous Institute from AY 2024-25, Affiliated to Savitribai Phule Pune University, Pune

**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester II

**Category: Program Core Laboratory 2**

**Course Code: VES2410P01** **Course Title: Laboratory Practice II**

| Teaching Scheme | | | | Evaluation Scheme | | | | |
|---|---|---|---|---|---|---|---|---|
| L | T | P | Cr | Exam | Theory % Marks | | Practical % Marks | |
| | | | | | Max | Min for Pass | Max | Min for Pass |
| 0 | 0 | 4 | 2 | CCA | - | - | 50 | 20 |
| Total Hours | | | | | - | - | | |
| 0 | 0 | 52 | Total: 52 | ESE | - | - | 50 | 20 |

**Prerequisites:**

1. Front End Tools and Back End Tools basics
2. C Language basics and Interfacing basics

**Course Objectives:**

1. To understand issues and tools related to Analog, Digital and Mixed signal design and implementation.
2. To design and develop models for various automotive control systems using model based development techniques.
3. To develop comprehensive approach towards building low cost and optimized area using FPGA/ASIC.
4. To enhance programming skills of students in the field of VLSI and Embedded systems.

**Course Outcomes:** After successful completion of the course the student will be able to:

| | |
|---|---|
| CO1 | Develop and Simulate various analog CMOS circuits for high frequency and high speed IC design. |
| CO2 | Design and implement various on chip circuits like Mod 4 counter on PLD. |
| CO3 | Implement programs to solve automotive well defined problems like ignition driver on an embedded platform. |
| CO4 | Design a Program for various applications like ADC, DAC in front end tool to analyze various output parameters voltage, current etc. using programming languages: Matlab, Python and C. |
| CO5 | Design a Program for various applications using back end tool to evaluate |

| | | |
|---|---|---|
| | parameters like VSWR using programming languages: Matlab, Python and C and Analyze and select Linux and Embedded Linux utilities with respect to real time applications. | |
| **Syllabus** | | |
| | **Introduction** | **02hrs** |
| Laboratory Practice II (LP II) is companion course of theory courses (core and elective) in Semester II. It is recommended that set of assignments or at least one study project per course is to be completed. Set of problem statements are suggested. Course/ Laboratory instructor may frame suitable problem statements. Student has to submit a report/Journal consisting of appropriate documents -prologue, Certificate, table of contents, and other suitable write up like (Introduction, motivation, aim and objectives, outcomes, brief theory, requirements analysis, design aspects, algorithms, mathematical model, complexity analysis, results, analysis and conclusions). | | |
| | **Guidelines for CCA** | **07 hrs** |
| Continuous assessment of laboratory work is done based on performance of student.<br>Each assignment/ mini project assessment is to be done based on parameters with appropriate weightage. Suggested parameters for overall assessment as well as mini project assessment include-timely completion, performance, innovation, efficient codes, usability, documentation and adhering to SDLC comprehensively | | |
| | **Guidelines for ESE** | **07 hrs** |
| It is recommended that examination should be conducted as presentation by student based on one of the mini projects completed and the content understanding of laboratory work. | | |
| **Lab practice file shall consist of following assignments/experiments** | | |
| **Guidelines:**<br>1. Total experiments to be conducted are two from each Part: Part A to Part D<br>2. Total: 08 experiments | | |
| **Detailed Syllabus:** | | |
| **Part A: Analog CMOS Design** | | **9 Hrs** |
| **Expt. No.** | **Title** | |
| 1. | To design a cascode current mirror for output current of 100 μA. Prepare layout and simulate. Comment on output resistance. | |
| 2. | To design, prepare layout and simulate CMOS differential amplifier for CMRR of 40 dB. Comment on ICMR. | |
| 3. | To design, prepare layout and simulate multistage CMOS RF amplifier in 90 nm technology for voltage gain of 60 dB, bandwidth of 100 MHz, and source impedance of 50 Ω. | |

**FY M Tech VLSI and Embedded Systems, Semester II**

<table>
<tr><td>4.</td><td>To design CMOS RF amplifier for voltage gain of 60 dB. Suggest and design suitable technique to enhance the bandwidth. Simulate each added technique step by step. Comment on the improvement resulted each time. Prepare layout of the final schematic and simulate.</td></tr>
<tr><td>5.</td><td>List the sources of cross talk. Explore in detail, the existence of cross talk in each case. Explain the mitigation techniques. Prepare case study for one of them. Verify the cross talk and its mitigation through simulation.</td></tr>
<tr><td colspan="2">Part B: System on Chip</td><td>9 Hrs</td></tr>
<tr><td>1.</td><td>Design, simulate and implement FSM on PLD for detection of either of input sequence X = … 1001.....or …1101… sequence and set output flags Y = “1“ or Z=“1“ respectively. What is the effect on area, speed, fan out and power by implementing this design using different state encoding styles?</td></tr>
<tr><td>2.</td><td>Design and implement MOD4 counter on PLD and verify multi-clock operations by probing logic analyzer<br>Control bits<br>Count update after every sec.
<table>
<tr><td>Control bits</td><td>Count update after every sec.</td></tr>
<tr><td>00</td><td>0.25 sec</td></tr>
<tr><td>01</td><td>0.5 sec</td></tr>
<tr><td>10</td><td>1 sec</td></tr>
<tr><td>11</td><td>4 sec</td></tr>
</table>
Why gated clock is not preferred in digital design? Write Verilog code to implement CMOS layout which will generate glitch also design a RTL by Write VHDL will generate glitch and also measure it using electronic test equipment.</td></tr>
</table>

**FY M Tech VLSI and Embedded Systems, Semester II**

| | | |
|---|---|---|
| 3. | Implement temperature logging system as a co-design by Interfacing FPGA &μC 8051 as follows:<br>i) LM 35 interfaced with ADC<br>ii) ADC interfaced with FPGA<br>iii) FPGA interfaced with μC 8051<br>iv) μC 8051 is interfaced with LCD | |
| 4. | To display real-time room temperature. If temperature is greater than 250 C Bi-colors LED should change its normal<br>Green color to RED color via opto-isolator by actuation of relay | |
| **Part C: Embedded Automotive Systems** | | **9 hrs** |
| 1. | Write a program for Sensing Engine Speed, Load and Temperature. | |
| 2. | Develop a transistorized Ignition Driver. | |
| 3. | Design a single cylinder engine Management System. | |
| 4. | Perform a case study for any two automotive protocols. | |
| 5. | Study the functional design aspects of Hybrid Automotive Systems. | |
| **Part D: Program Elective course experiments** | | **9 hrs** |
| **Embedded Product Design** | | |
| 1. | To estimate techno-commercial feasibility of any one embedded product such as mobile phone, programmable calculator, tablet PC, biometrics system, set top box etc. | |
| 2. | To study design considerations of any one embedded product e.g. laptop, video conferencing system, surveillance/ security system, EMG/ECG machine etc. | |
| 3. | To design any one embedded product to solve any real life problems. | |
| 4. | To test the hardware designed for above assignment (3) using a suitable simulation tool. | |
| 5 | To simulate the software designed for the above assignment (3) using suitable simulation tool. | |
| **High Speed ICs** | | |
| 1. | Simulate RC circuit and comment on transient response. | |

**FY M Tech VLSI and Embedded Systems, Semester II**

| | |
|---|---|
| 2. | Simulate startup model of RLC. |
| 3. | Simulate a transmission line to evaluate VSWR, reflection coefficient parameters considering different loading considerations using analog simulation tool. |
| 4. | Plot stability circle, for given values of S parameters. |
| **Mixed Signal IC Design** | |
| 1. | Plot ideal transfer curves for 3 bit and 4 bit DAC, using VRef = 5V and 3V. Find the resolution for a DAC if the output voltage is desired to change in 1 mV increments. |
| 2. | For 3 bit ADC, VRef = 5V, Plot ideal transfer curve and quantization error. |
| 3. | Plot transfer curve and quantization error by shifting entire transfer curve of example 2, left by 1/2 LSB and calculate DNL. |
| 4. | Design and simulate anti-aliasing filter with two input sine waves having frequencies 4 MHz and 40 MHz. |
| 5. | Design and simulate sample and hold circuit, with 8 MHz sine wave sampled at 100 MHz. |
| **Embedded Signal Processor Architectures** | |
| 1. | Design and simulate N point FFT by targeting DSP processor platform. |
| 2. | Design and simulate N tap FIR filter by targeting suitable DSP processor platform. |
| 3. | Design and simulate LMS adaptive filter. |
| 4. | Design a system for DTMF signal detection. Write a program to detect the DTMF signal using Goertzel algorithm |
| **Real Time Operating Systems** | |
| 1. | Multitasking in µCOS- II RTOS using minimum 3 tasks on ARM7. (µCOS - II based Experiments). |
| 2. | Semaphore as signaling and synchronizing on ARM7. (µCOS - II based Experiments). |
| 3. | Write a program for 4*4 Matrix Keypad Interface ( based on Linux Operating System). |
| 4. | Develop character device driver for GPIO (based on Linux Operating System). |

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**Department of Electronics and Telecommunication**

**FY M Tech VLSI and Embedded Systems, Semester II**
**Rubrics for Continuous Evaluation**

| Component | Level | Laboratory Practice II | Total | Passing | Process Evaluation |
|---|---|---|---|---|---|
| Continuous Comprehensive Assessment (CCA) | Faculty | 1. Dynamics & Vibrations<br>2. Design & Optimization<br>3. Finite Element Techniques | 50 | 20 | Refer CCA Guideline |
| ESE | Institute | | 50 | 20 | External Oral Examination |

**CO-PO Mapping**

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 3 | 2 | 2 | 2 | 1 | 1 |
| **CO2** | 3 | 2 | 2 | 2 | 1 | 1 |
| **CO3** | 3 | 2 | 2 | 2 | 1 | 1 |
| **CO4** | 2 | 1 | 1 | 1 | 1 | 1 |
| **CO5** | 1 | 1 | 1 | 1 | 1 | 1 |

3: High, 2: Moderate, 1: Low, 0/-: No Mapping

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# D Y Patil College of Engineering, Akurdi, Pune

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester II

**Category: Credit Course**

**Course Code: VES2410P02** **Course Title: Skill Development Course**

| Teaching Scheme | | | | Evaluation Scheme | | | | |
|---|---|---|---|---|---|---|---|---|
| L | T | P | Cr | Exam | Theory % Marks | | Practical % Marks | |
| | | | | | Max | Min for Pass | Max | Min for Pass |
| 0 | 0 | 4 | 2 | CCA | - | - | 100 | 40 |
| 0 | 0 | 52 | Total:52 | | | | | |

**Prerequisites**: NIL

**Course Objectives:** Purposes of Course are:

1. Enhance Technical Expertise: Equip students with advanced technical skills and knowledge in their specific field of study, enabling them to solve complex engineering problems and contribute to innovative solutions.
2. Industry-Relevant Skills: Bridge the gap between academic knowledge and industry requirements by providing training in the latest tools, technologies, and methodologies used in the industry, ensuring students are job-ready upon post-graduation.
3. Professional Development: Develop essential soft skills such as leadership, teamwork, communication, and project management, preparing students for leadership roles in their professional careers and enhancing their overall employability.

**Course Outcomes:** After Successful completion of course units, students will

| | |
|---|---|
| CO1 | Demonstrate advanced technical skills and practical knowledge in their specialized field, enabling them to effectively design, analyze, and implement complex engineering solutions using industry-standard tools and technologies. |
| CO2 | Exhibit strong professional skills, including effective communication, teamwork, and project management, preparing them to lead and collaborate in multidisciplinary teams within a dynamic work environment. |

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester II

**Syllabus**

| **Unit I** | **Modern Tools** | **26 hrs** |
|---|---|---|

Overview of current Industry trends in Latest and Modern Software/Gadget/Equipment/Concept/Procedure/Tools, Hands on Training, Integrating these tools for comprehensive solutions. Applications of software.

| **Unit II** | **Professional and Technical Communication** | **26 hrs** |
|---|---|---|

Understanding the importance of professional and technical communication, Key elements of effective communication, Hands on writing technical reports, research papers, and documentation. Structuring and formatting technical documents. Clarity, conciseness, and coherence in technical writing. Use of visual aids (charts, graphs, diagrams) in documents. Preparing and delivering technical presentations. Public speaking skills for technical contexts.

Effective use of presentation tools (e.g., PowerPoint, Canva). Communicating within a team and with stakeholders. Conducting and participating in technical meetings and discussions.

Listening skills and feedback mechanisms. Effective email communication. Utilizing digital platforms for collaboration and communication (e.g., Zoom, Microsoft Teams).

**References:**


1. "Technical Communication: Principles and Practice" by Meenakshi Raman and Sangeeta Sharma, Oxford University Press, Third Edition, 2015, New Delhi
2. "Professional Communication" by Aruna Koneru,Tata McGraw-Hill Education, Second Edition, 2008, New Delhi
3. "Effective Technical Communication" by M. Ashraf Rizvi, Tata McGraw-Hill Education, Second Edition, 2010, New Delhi
4. "Communication Skills for Engineers" by Sunita Mishra and C. Muralikrishna, Pearson Education India, First Edition, 2011, New Delhi
5. "Advanced Technical Communication" by Kavita Tyagi and Padma Misra, PHI Learning Pvt. Ltd., First Edition, 2011, New Delhi

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester II
## Rubrics for Continuous Evaluation

| Component | Level | Unit 1 | Unit 2 | Total | Passing | Process Evaluation |
|---|---|---|---|---|---|---|
| Continuous Comprehensive Assessment (CCA) | Faculty | 50 | 50 | 100 | 40 | Refer CCA Guideline |

## CO-PO Mapping

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 3 | 2 | 3 | 2 | - | 3 |
| **CO2** | 3 | 2 | - | 3 | 3 | 3 |

3: High, 2: Moderate, 1: Low, 0/-: No Mapping

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# D Y Patil College of Engineering, Akurdi, Pune

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**Department of Electronics and Telecommunication**

**FY M Tech VLSI and Embedded Systems, Semester II**

**Category: Credit Course**

**Course Code: VES2410P03** **Course Title: Industry Based Mini Project**

| Teaching Scheme | | | | Evaluation Scheme | | | | |
|---|---|---|---|---|---|---|---|---|
| L | T | P | Cr | Exam | Theory % Marks | | Practical % Marks | |
| | | | | | Max | Min for Pass | Max | Min for Pass |
| 0 | 0 | 4 | 2 | CCA | | | TW 50 | 40 |
| 0 | 0 | 52 | Total: 52 | | | | OR 50 | 40 |

Industry Based Mini Project involves students working on real-world projects in collaboration with industry partners. This course provides practical experience, allowing students to apply theoretical knowledge to solve industry-specific problems. It includes regular mentoring sessions, project planning, execution, and final presentations. By the end of the course, students gain valuable insights into industry practices, enhance their technical and professional skills, and improve their employability.

**Prerequisites**: Knowledge of Statistics, problem solving approach.

**Course Objectives:**

1. To gain practical insights into Industry specific practices, challenges and standards.
2. To develop critical thinking by aligning complexities of Industrial Environment.

**Course Outcomes:** After successful completion of the course the student will be able to

| | |
|---|---|
| CO1 | Design, plan and execute the project which provides a viable solution or improvement related to existing solutions. |
| CO2 | Author findings and solution effectively through written reports and oral presentation. |

**Syllabus**

Task 1: Explore domain specific industry websites to identify relevant projects.

Task 2: Prepare project plan involving problem statement, objectives, methodology, intended outcomes.

Task 3: Conduction and deliver progress review presentations with results and discussions.

Task 4: Preparation and presentation of final Mini project report

## FY M Tech VLSI and Embedded Systems, Semester II

**References**


- Kerzner, H. (2017). Project management: A systems approach to planning, scheduling, and controlling (12th ed.). Wiley.
- Kerzner, H. (2017). Project management case studies (5th ed.). Wiley
- Smith, N. J. (2019). Engineering project management (4th ed.). Wiley-Blackwell
- Oberlender, G. D. (2014). Project management for engineering and construction (3rd ed.). McGraw-Hill Education.


### Rubrics for Continuous Evaluation

| Component | Level | Industry Based Mini Project | Total | Passing | Process Evaluation |
|---|---|---|---|---|---|
| Continuous Comprehensive Assessment (CCA) | Faculty | Mini project Report | 50 | 20 | Refer CCA Guideline |
| ESE | Department | Mini project Presentation | 50 | 20 | Refer Guidelines |

### CO-PO Mapping

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 2 | 2 | 2 | 3 | 2 | 3 |
| **CO2** | 3 | 2 | 2 | 3 | 2 | 3 |

3: High, 2: Moderate, 1: Low, 0: No Mapping

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# D Y Patil College of Engineering, Akurdi, Pune

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**Department of Electronics and Telecommunication**

**FY M Tech VLSI and Embedded Systems, Semester II**

**Category: Non Credit Course 2**

**Course Code: NCC2410L01** **Course Title: Stress Management by Yoga**

| Teaching Scheme | | | | Evaluation Scheme | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| L | T | P | Cr | Exam | Theory % Marks | | | Practical % Marks | |
| | | | | | Max | Min for Pass | | Max | Min for Pass |
| 2 | 0 | 0 | 0 | CCA | 100 | 40 | 40 | - | - |
| 26 | 0 | | Total:26 | | | | | | |

**Prerequisites:** Familiarity with Basic Yoga Practices, General Physical Fitness

**Course Objective:**

1. To provide students with a thorough understanding of stress, its causes, and its effects on mental and physical health.
2. To teach students various yoga practices, including asanas, pranayama, and meditation, for stress management and overall well-being.
3. To enable students to incorporate the philosophical principles of yoga into their daily routines to enhance mental and physical well-being.

**Course Outcomes:** After successful completion of the course the student will be able to

| | |
|---|---|
| CO1 | Comprehend stress sources and yoga's role. |
| CO2 | Demonstrate mastery in yoga techniques. |
| CO3 | Apply yoga philosophy to stress management. |
| CO4 | Incorporate yoga for long-term well-being. |

**Syllabus**

| Unit I | Introduction to Stress and Yoga | 7 |
|---|---|---|

*Understanding Stress:* Types, causes, and impacts

*Introduction to Yoga:* Definition, history, and paths (Raja, Karma, Bhakti, Jnana)

*Connection between Stress and Yoga:* role of Yoga in stress reduction

| Unit II | Yoga Practices for Stress Management | 7 |
|---|---|---|

*Asanas (Postures):* Basic stress-relieving asanas (e.g., Shavasana, Balasana)

*Pranayama (Breathing Techniques):* Techniques like AnulomVilom, Bhramari, Nadi Shodhana

*Meditation and Relaxation:* Mindfulness meditation, guided imagery, progressive relaxation

**FY M Tech VLSI and Embedded Systems, Semester II**

| | | |
|---|---|---|
| **Unit III** | **Philosophical Foundations of Yoga** | **6** |

*Yoga Philosophy:* Eight limbs of yoga

*Mind-Body Connection:* Psychosomatic health in yoga

*Lifestyle and Diet:* Yogic lifestyle, Sattvic diet

| | | |
|---|---|---|
| **Unit IV** | **Applied Yoga for Stress Management** | **6** |

*Yoga Therapy:* Personalized yoga routines for stress

*Case Studies:* Real-life applications and analysis

*Integrating Yoga into Daily Life:* Practical tips for daily practice

**Reference Books**

**Text Books**


1. The Yoga Sutras of Patanjali, by Swami Satchidananda
2. Light on Yoga, by B.K.S. Iyengar
3. The Heart of Yoga, by T.K.V. Desikachar


**Reference Books**


Journals and Articles: International Journal of Yoga, Journal of Alternative and Complementary Medicine


**Web References**

Yoga Alliance

International Association of Yoga Therapists National Portal of India

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester II
## Rubrics for Continuous Evaluation

| Component | Level | Unit 1 | Unit 2 | Unit 3 | Unit 4 | Total | Passing | Process Evaluation |
|---|---|---|---|---|---|---|---|---|
| Continuous Comprehensive Assessment (CCA) | Faculty | 25 | 25 | 25 | 25 | 100 | 40 | Refer CCA Guideline |

### CO-PO Mapping

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 2 | 2 | 2 | 3 | 1 | 2 |
| **CO2** | - | 2 | 2 | - | 2 | 3 |
| **CO3** | 2 | 1 | 2 | 2 | - | 3 |
| **CO4** | 2 | - | 3 | 2 | 2 | - |

3: High, 2: Moderate, 1: Low, 0: No Mapping

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# D Y Patil College of Engineering, Akurdi, Pune

An Autonomous Institute from AY 2024-25, Affiliated to Savitribai Phule Pune University, Pune

**Department of Electronics and Telecommunication**

**FY M Tech VLSI and Embedded Systems, Semester II**

**Category: Non Credit Course 2**

**Course Code: NCC2410L02 Course Title: Personality Development through Life Enlightenment Skills**

| Teaching Scheme | | | | Evaluation Scheme | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| L | T | P | Cr | Exam | Theory % Marks | | | Practical % Marks | |
| | | | | | Max | Min for Pass | | Max | Min for Pass |
| 2 | 0 | 0 | 0 | CCA | 100 | 40 | 40 | - | - |
| 26 | 0 | | Total:26 | | | | | | |

**Prerequisites:**

1. Basic Anatomy and Physiology
2. Introduction to Psychology
3. Familiarity with Basic Yoga Practices
4. General Physical Fitness
5. Interest in Holistic Health Approaches

**Course Objective :**

1. To cultivate essential skills that contribute to personal development and self-awareness.
2. To train students with the tools and techniques necessary for professional growth and career advancement.
3. To foster a balanced approach to life by integrating principles that support physical, mental, and emotional well-being.

**Course Outcomes:** After successful completion of the course the student will be able to

| | |
|---|---|
| CO1 | Understand and reflect on their own values, beliefs, and emotions, fostering greater emotional intelligence for personal and professional contexts. |
| CO2 | Develop students ability to communicate effectively in various settings and build strong, empathetic relationships through advanced interpersonal techniques. |
| CO3 | Prepare students to lead with confidence and integrity, understanding different leadership styles and enhancing their ability to work effectively in teams and solve problems collaboratively. |
| CO4 | Encourage a commitment to lifelong learning and ethical conduct, providing strategies for career advancement, personal branding, and continuous self-improvement. |

# D Y Patil College of Engineering, Akurdi, Pune

An Autonomous Institute from AY 2024-25, Affiliated to Savitribai Phule Pune University, Pune

**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester II

### Syllabus

| | | |
|---|---|---|
| **Unit I** | **Self-Awareness and Emotional Intelligence** | **7** |

*Understanding Self:* Exploration of self-concept, values, and beliefs to cultivate self-awareness.

*Emotional Intelligence (EI):* Development of EI competencies including self-awareness, self-regulation, empathy, and social skills.

*Self-Management:* Techniques for setting and achieving personal goals, managing time effectively, and coping with stress.

| | | |
|---|---|---|
| **Unit II** | **Communication and Interpersonal Skills** | **7** |

*Effective Communication:* Principles of clear and persuasive communication, including verbal, non-verbal, and written communication.

*Interpersonal Relationships:* Strategies for building and maintaining healthy relationships, conflict resolution, and active listening.

*Public Speaking:* Techniques to overcome stage fright, structure engaging speeches, and captivate an audience.

| | | |
|---|---|---|
| **Unit III** | **Leadership and Teamwork** | **6** |

*Leadership Styles:* Exploration of different leadership styles such as transformational, transactional, and servant leadership.

*Team Dynamics:* Understanding group behavior, fostering collaboration, and resolving conflicts within teams.

*Decision Making and Problem Solving:* Development of critical thinking skills, decision-making models, and problem-solving strategies.

| | | |
|---|---|---|
| **Unit IV** | **Personal Growth and Professional Development** | **6** |

*Career Planning:* Tools and techniques for setting career goals, personal branding, and navigating the job market.

*Continuous Learning:* Strategies for lifelong learning, staying abreast of industry trends, and acquiring new skills.

*Ethics and Values:* Exploration of ethical considerations in professional contexts, integrity, and responsible citizenship.

**Reference Books**

**Text Books**


1. Emotional Intelligence 2.0, by Travis Bradberry and Jean Greaves
2. How to Win Friends and Influence People, by Dale Carnegie
3. The 7 Habits of Highly Effective People, by Stephen R. Covey
4. Leaders Eat Last, by Simon Sinek

## FY M Tech VLSI and Embedded Systems, Semester II

**Reference Books**

Journals and Articles:

Journal of Personality and Social Psychology

Harvard Business Review

**Web References**

TED Talks on leadership, communication, and personal development

Harvard Business Review articles on emotional intelligence and leadership

### Rubrics for Continuous Evaluation

| Component | Level | Unit 1 | Unit 2 | Unit 3 | Unit 4 | Total | Passing | Process Evaluation |
|---|---|---|---|---|---|---|---|---|
| Continuous Comprehensive Assessment (CCA) | Faculty | 25 | 25 | 25 | 25 | 100 | 40 | Refer CCA Guideline |

### CO-PO Mapping

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 3 | - | 3 | 3 | 1 | 2 |
| **CO2** | 3 | 3 | 2 | - | 2 | 3 |
| **CO3** | 3 | 1 | 2 | 2 | - | 3 |
| **CO4** | 3 | 3 | - | 2 | 2 | 2 |

3: High, 2: Moderate, 1: Low, 0: No Mapping

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**Department of Electronics and Telecommunication**

**FY M Tech VLSI and Embedded Systems, Semester II**

**Category: Non Credit Course 2**

**Course Code: NCC2410L03** **Course Title: Intellectual Property Rights (IPR)**

| Teaching Scheme | | | | Evaluation Scheme | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| L | T | P | Cr | Exam | Theory % Marks | | | Practical % Marks | |
| | | | | | Max | Min for Pass | | Max | Min for Pass |
| 2 | 0 | 0 | 0 | CCA | 100 | 40 | 40 | - | - |
| 26 | 0 | | Total:26 | | | | | | |

**Prerequisites:**

Students should have a foundational understanding of legal principles, a strong technical background in their field, research and analytical skills, and proficiency in communication.

**Course Objective:**

1. To provide students with a comprehensive understanding of the basics of intellectual property rights, including patents, trademarks, copyrights, and trade secrets.
2. To educate students on the legal frameworks governing IPR and the detailed procedures involved in securing patents.
3. To engage students in the examination of current issues and challenges in the field of intellectual property rights, particularly in relation to technology and innovation.

**Course Outcomes:** After successful completion of the course the student will be able to

| | |
|---|---|
| CO1 | Explain the fundamental concepts and significance of various types of intellectual property rights. |
| CO2 | Gain the ability to navigate the patent application process, conduct patent searches, and understand patent infringement and litigation procedures. |
| CO3 | Acquire the skills to register, protect, and enforce trademarks and copyrights, including understanding their digital applications. |
| CO4 | Develop an understanding of current and emerging trends in IPR, including issues related to trade secrets, biotechnology, competition law, and the impact of new technologies. |

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**Department of Electronics and Telecommunication**

**FY M Tech VLSI and Embedded Systems, Semester II**
**Syllabus**

| **Unit I** | **Introduction to Intellectual Property Rights** | **6** |
|---|---|---|

*Fundamentals of Intellectual Property:* Definition and nature of intellectual property, Importance of intellectual property in innovation and technology, Types of intellectual property: patents, trademarks, copyrights, trade secrets.

*International Framework for Intellectual Property:* Overview of international IPR agreements (TRIPS, WIPO), Role of international organizations in IPR, Comparison of IPR laws in different countries.

*Intellectual Property Laws in India:* Historical background of IPR laws in India, Key IPR legislations in India (Patent Act, Trademark Act, Copyright Act, etc.), Government bodies and agencies involved in IPR protection and enforcement.

| **Unit II** | **Patents** | **8** |
|---|---|---|

*Basics of Patents:* Definition and criteria for patentability, Types of patents (utility patents, design patents, plant patents), Patent application process and documentation.

*Patent Search and Analysis:* Techniques for conducting patent searches, Tools and databases for patent information, Patent mapping and analysis for research and development.

*Patent Infringement and Litigation:* Understanding patent infringement, Remedies for patent infringement (legal actions, damages), Case studies of patent infringement and litigation.

*Patent Licensing and Commercialization:* Strategies for patent licensing and technology transfer, Valuation of patents and negotiation techniques, Case studies on successful patent commercialization.

| **Unit III** | **Trademarks and Copyrights** | **6** |
|---|---|---|

*Trademarks:* Definition and types of trademarks, Process of trademark registration, Protection of trademark rights and enforcement, Case studies on trademark disputes and resolutions.

*Copyrights:* Definition and scope of copyrights, Works eligible for copyright protection, Process of copyright registration, Copyright infringement and remedies.

*Digital Intellectual Property:* Protection of intellectual property in the digital age, Issues related to digital rights management (DRM), Legal aspects of software and internet-related intellectual property.

| **Unit IV** | **Emerging Trends and Issues in IPR** | **6** |
|---|---|---|

*Trade Secrets and Confidential Information:* Definition and importance of trade secrets, Protection of trade secrets, Legal remedies for misappropriation of trade secrets.

*IPR and Competition Law:* Interaction between IPR and competition law, Anti-competitive practices and abuse of IPR, Case studies on IPR and competition law conflicts.

*Current Trends and Future Directions:* Impact of artificial intelligence and machine learning on IPR, IPR issues in emerging technologies (nanotechnology, IoT), Future trends in IPR protection and management..

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**Department of Electronics and Telecommunication**

## FY M Tech VLSI and Embedded Systems, Semester II

### Books

**Text Books**

1. Intellectual Property Rights: Unleashing the Knowledge Economy, by Prabuddha Ganguli
2. Intellectual Property: The Law of Trademarks, Copyrights, Patents, and Trade Secrets, by Deborah E. Bouchoux
3. Patent Law and Policy: Cases and Materials, by Robert Patrick Merges, John Fitzgerald Duffy
4. The Law of Intellectual Property, by Craig Allen Nard, Michael J. Madison, and Mark P. McKenna

**Reference Books**

1. Intellectual Property Rights in the Global Economy, by Keith E. Maskus
2. Intellectual Property and Business: The Power of Intangible Assets, by Rodney D. Ryder

### Web References

1. https://onlinecourses.nptel.ac.in/noc22_hs59/preview
2. https://archive.nptel.ac.in/courses/110/105/110105139/
3. https://dst.gov.in/sites/default/files/E-BOOK%20IPR.pdf

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## FY M Tech VLSI and Embedded Systems, Semester II
## Rubrics for Continuous Evaluation

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| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 |
|---|---|---|---|---|---|---|
| **CO1** | 3 | 3 | 3 | 2 | - | 2 |
| **CO2** | - | 3 | 2 | 2 | 2 | 3 |
| **CO3** | 3 | 2 | 2 | 2 | 3 | - |
| **CO4** | 3 | 3 | - | 2 | 2 | 2 |

3: High, 2: Moderate, 1: Low, 0: No Mapping

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